MIXED SIGNAL CIRCUIT DESIGN ORAL NOTES

Guide to these notes:

- If you payed for these notes, **you've been scammed**. I always give my notes for free.
- I tried to explain and justify every step of each question, I hope you can follow my reasonings. If there's something that's "taken for granted", it means it was discussed in previous courses (i.e: fundamentals of electronics or analog circuit design)
- Even though the oral hasn't a list of questions to be asked, I made one. It was handy to me.
- PDFs contain typos so beware of that!
- Tip: do not go straight to the point during the oral. When you're asked a question give context. It does not make sense to start talking about the circuit implementation of a BGR if you first didn't explain what principle (positive/negative temperature coefficient combination) is behind that. It also does not make sense to explain how to design a Common Mode Feedback circuit if you don't know why it's there (i.e: fully differential circuits simply DO NOT WORK without that, CMF isn't used just to reduce the common mode gain, that's just a pleasant consequence). This will also help you structuring the oral
- if my writing isn't clear, well, I'm sorry C: hope it helps anyway. Also, I speak maccheroni and I'm well aware of the English mistakes I made. My priority was to have a clear understanding of the topics.
- At some point the index number of a question in the scanned document does not reflect the one of the table of contents. Nevermind, use bookmarks and the real pages!

If you're having any issue with this document just send an email to
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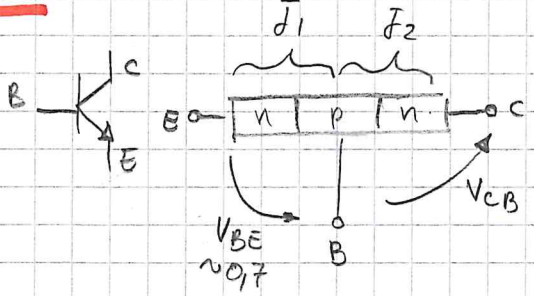
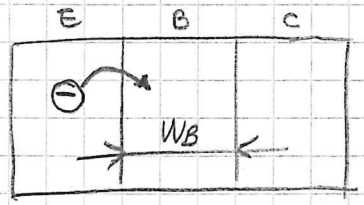
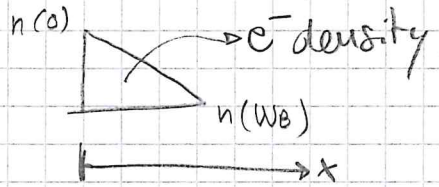
1) Review of BJT devices

NPN





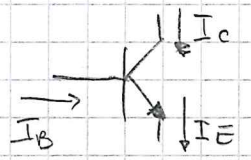


Base (p type) is very narrow and J_1 is forward biased $\sim 0,7V$

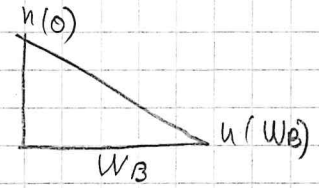
We assume that $V_{CB} > 0$ thus J_2 is reverse biased → collector "collects" the electrons

1st approximation: since the base is thin, all e^- are collected through the collector.

What about current I_B? Some holes are injected in the emitter, others are recombined with electrons in the base region.



$$J_n = q D_n \frac{n(0)}{W_B}$$ → e^- density @ $x=0$



$$= q \frac{D_n}{W_B} \frac{n_i^2}{N_B} e^{V_{BE}/V_{TH}}$$ where $V_{TH} = \frac{kT}{q} \sim 25,8\ mV$ @300K

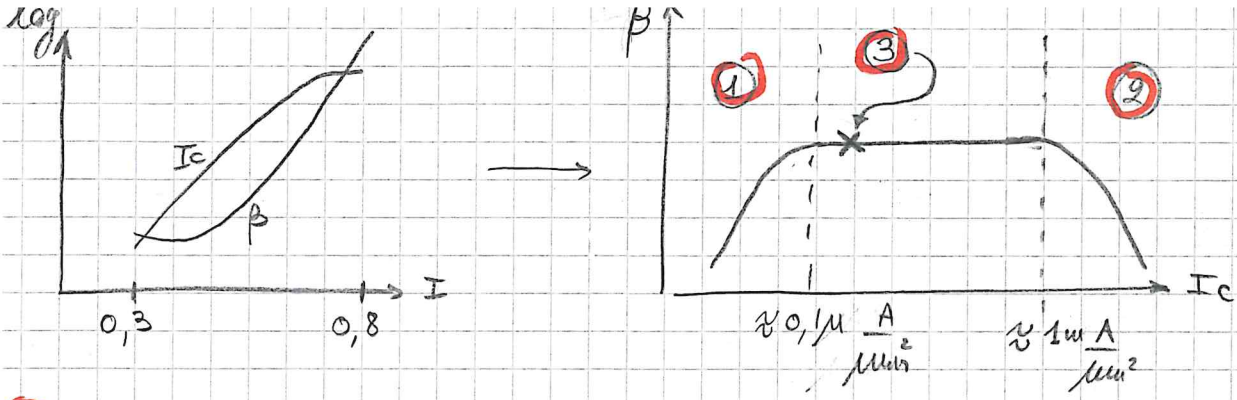
Note that n_i^2 heavily depends on temperature

$I_C = J_n A \simeq I_S e^{V_{BE}/V_{TH}}$ → exp relation → to increase I_C by 10, we'd just need $\sim 60mV$ more on V_{BE}

$I_E = I_C + I_B$ → def $\alpha \triangleq \frac{I_C}{I_E} = 0,989...$

$\frac{I_C}{\alpha} = I_C + I_B \rightarrow I_C = I_B \left(\frac{\alpha}{1-\alpha}\right) = \beta I_B$ where $\beta \sim 100 \div 250$

Remember that β changes with current level:



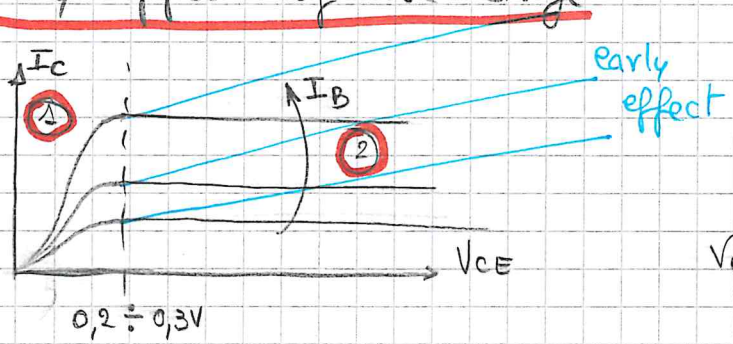
(2) I_C too large → base increases in width → β drops

(1) I_C too small → recombination at the base is too relevant → β drop

(3) Typical I_C bias point because:

- Going into (1) means too low power → smaller risk compared to (2)
- Biasing at lowest I_C is optimal for increasing R_π
  (so the motivation is to increase input impedance of the stage)

Early effect of the stage



(1) Saturation region

(2) Active region

$r_O = V_A / I_C$

Early effect: if V_{CE} ↗ then V_{CB} ↗ → W_B ↗

Remember that r_o is not a physical resistor → it's the mathematical representation of the ΔI with ΔV_{CE} → NOT NOISY!

Transconductance

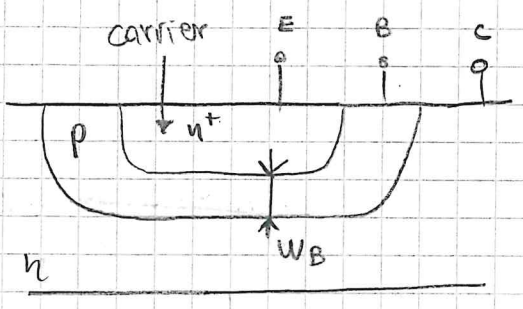
$$\frac{\Delta I_C}{\Delta V_{BE}} \Rightarrow \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{V_{TH}} = g_m$$

Typically, small distortion is achieved with $\Delta V_{BE} \ll V_{TH}$

Note: $g_m|_{BJT} > g_m|_{MOS}$ ⇝ it usually is larger

PNP

Unlike pMOS devices, pnp bipolar are not complementar w.r.t npn pnp performance is much worse compared to the one of npn. Why? Because of the physical implementation:

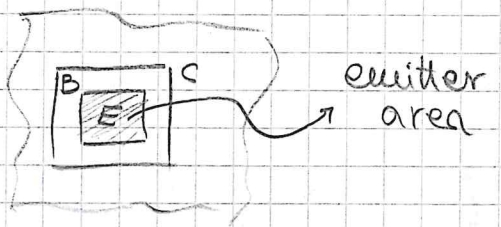


↳ NPN: vertical flow of the current in a small size compared to MOS. Remember that MOS current flows in a thin sheet of charge → large C_p

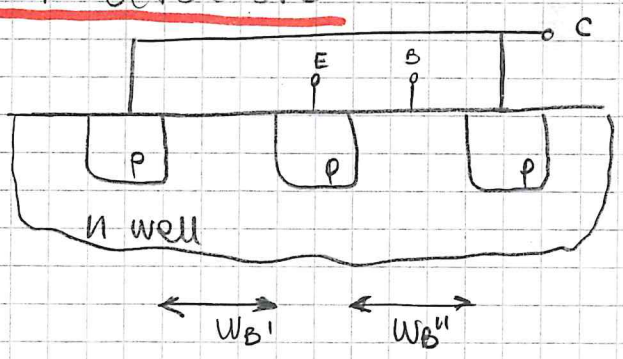
W_B of an NPN is not easy to control because of etching

Note that we have a physical resistance connecting E-C.

Top view:



PNP structure



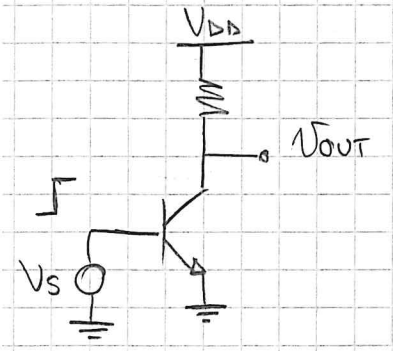
↳ lateral transistor → larger size compared to npn.

β lower because of larger W_B.

ω_T (cut off frequency) is lower as well for this reason.

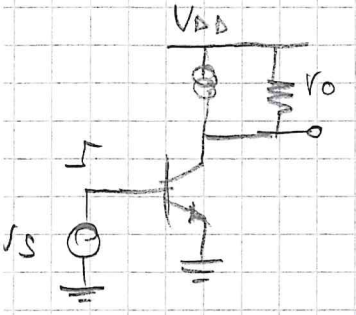
W_B is larger because the process is optimized for vertical technology (i.e: npn implementation)

2) Basic BJT amplifiers, impedances and cutoff frequency



$$v_{OUT} = -g_m v_s R_L = -\frac{I_C}{V_{TH}} R_L v_s = \frac{V_R}{V_{TH}} v_s$$

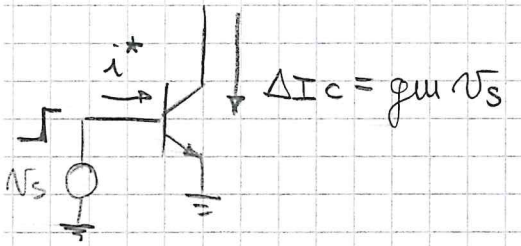
We can increase the gain with an active load.



$$G = -g_m r_o = -\frac{\cancel{I_C}}{V_{TH}} \cdot \frac{V_A}{\cancel{I_C}} = -\frac{V_A}{V_{TH}} = -\mu_V \sim -1000 \div 400$$

Note that $\mu_{BJT} \gg \mu_{MOS}$

What about base current?



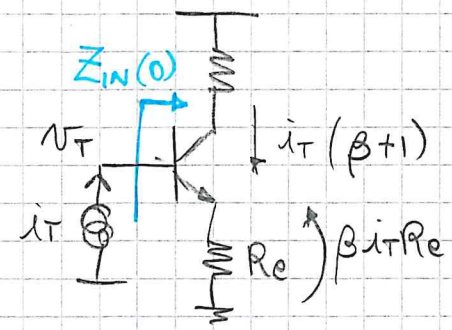
$$i^* = g_m v_s \cdot \frac{1}{\beta} = \Delta I_B$$

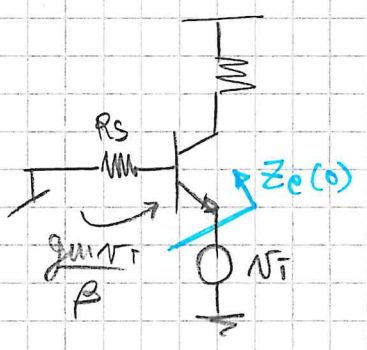
ΔI_c, ΔI_B are in phase → resistive behaviour

$$\frac{v_s}{\Delta I_B} = \frac{\beta}{g_m} = r_\pi$$ → unthewntical model → NOT a physical resistor

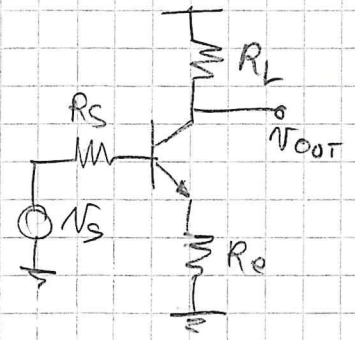
We use low I_C bias in order to have $1/g_m$ ↘ so r_π ↗

Base / collector impedance





$$Z_{IN}(0) = \frac{v_T}{i_T} = r_\pi + \beta R_E$$



$$G = \frac{V_{OUT}}{V_S} = -R_L \cdot \frac{1}{\frac{1}{g_m} + R_e + \frac{R_S}{\beta}} \overset{(1)}{\approx} -\frac{R_L}{R_e}$$

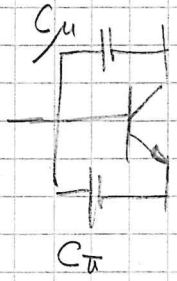
(1) is valid for large β and $g_m R_e \gg 1$

Where $g_m R_e$ is the local loop gain G_{loop} of the degeneration

$g_m R_e = \frac{I_C}{V_{TH}} R_e \longrightarrow g_m R_e = \frac{V_e}{V_{TH}}$ ~ Bias voltage of R_e

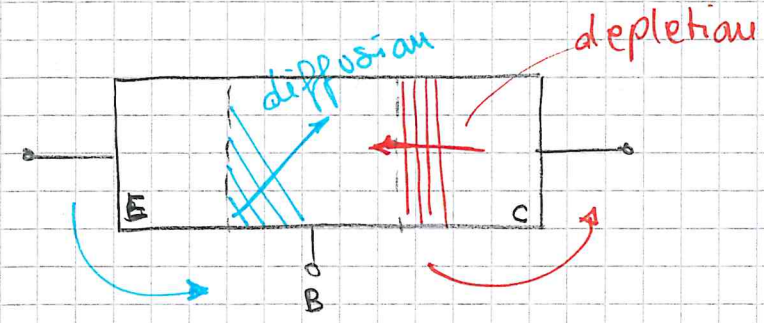
So, in order to check if degeneration is good we only need to check that $V_e \gg V_{TH}$

Parasitic capacitance



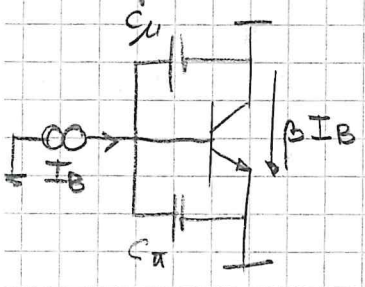
C_μ: depletion modulation capacitance
C_π: carrier modulation capacitance

C_μ is usually problematic because of the Miller effect and it comes from the depletion region in the base



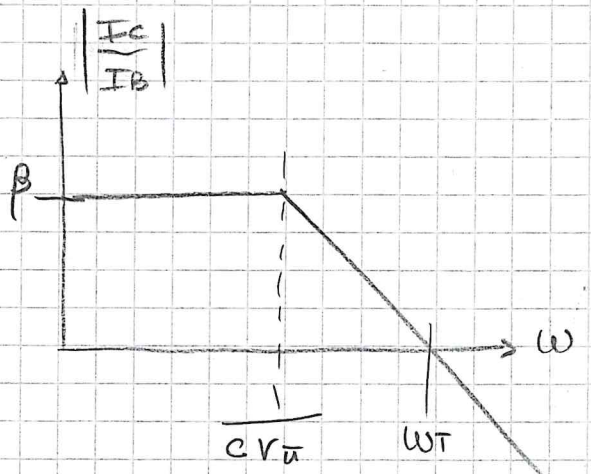
Cutoff frequency ω_T

Setup this measurement circuit



$$C_{TOT} = C_\mu + C_\pi = C$$

$$i_c = g_m i_B \frac{\frac{1}{sC} r_\pi}{\frac{1}{sC} + r_\pi}$$

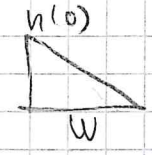


$$\frac{i_c}{i_B} = \frac{\beta}{1 + sC r_\pi} \qquad \tau = \frac{1}{(C_\mu + C_\pi)\beta/g_m}$$

$$\omega_T = \frac{g_m}{C_\pi + C_\mu} = \frac{1}{\frac{C_\pi}{g_m} + \frac{C_\mu}{g_m}}$$

Note, C_π and C_μ change with current so increasing I_c will not increase ω_T:

$$I_c = q D_n A \frac{n(0)}{W_B} \qquad Q = q \frac{AW}{2} n(0)$$ ↝ Area of triangle



$$\tau_{DIFF} = \frac{Q}{I_c} = \frac{W_B^2}{2 D_n} = \frac{W_B^2}{2 \mu_n \frac{KT}{q}}$$

$$C_\pi = \frac{dQ}{dV_{BE}} \qquad g_m = \frac{dI_c}{dV_{BE}} \quad \rightarrow \quad \frac{C_\pi}{g_m} = \frac{dQ}{dI_c} = \tau_{DIFF}$$ (1)

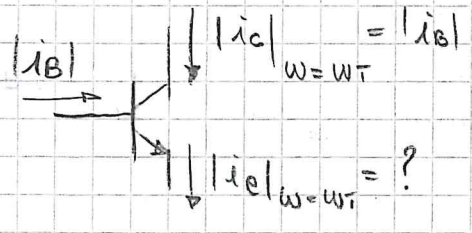
(1) It means that it does not depend on bias but on tech only

To first order, we can consider C_μ to be negligible with bias, so:

$$\omega_T = \frac{1}{\frac{C_\pi}{g_m} + \frac{C_\mu}{g_m}} = \frac{1}{\tau_{DIFF}} = \frac{2 \mu_n \frac{KT}{q}}{W_B^2}$$

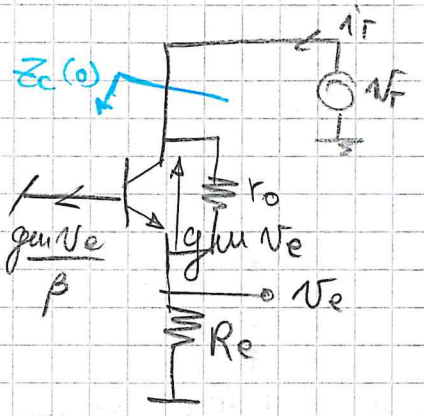
$\frac{C_\mu}{g_m}$ → NEG with bias

Note:



At $\omega = \omega_T$ what's the i_e value? One would be tempted to say $2 i_B$ but it can't be possible. We have the 90° phase shift between i_c, i_B because of the capacitors

Impedance on collector



$$\begin{cases} i_T = \frac{v_E}{R_e} + \frac{g_m v_e}{\beta} \\ i_T = \frac{v_T - v_e}{r_o} - g_m v_e \end{cases}$$

$$\rightarrow Z_c(0) = \frac{v_T}{i_T} = r_o \left[1 + \frac{\beta R_e}{r_o} \left(\frac{1 + g_m r_o}{\beta + g_m R_e} \right) \right]$$

Typically $g_m r_o \gg 1$ so

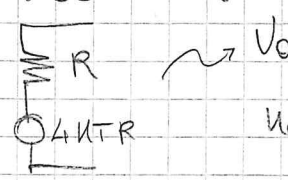
$$Z_c(0) = \frac{v_T}{i_T} \approx r_o \left[1 + \frac{g_m R_e}{1 + R_e/\pi} \right]$$

If $R_e \gg \beta/g_m \rightarrow Z_c(0) \approx r_o (1+\beta) \approx r_o \beta$

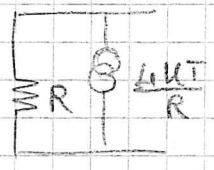
Note: cascoded BJTs are basically useless because it's not useful to have hard degeneration on bipolars (see later)

5) Noise in bipolar analog stages

- To reduce noise, we typically increase the power (see later)
- We'll always have poles that filter noise
- ∞ noise cannot exist because we would have ∞ power otherwise



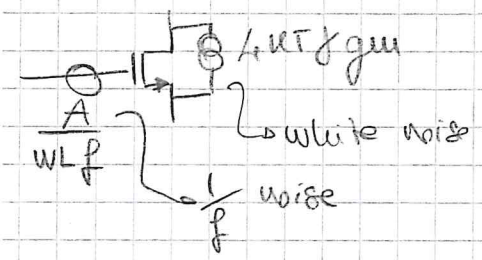
Voltage eq. noise



Current eq noise

Is 1MΩ noisier than 50Ω? It depends on the noise considered
(voltage noise → 50Ω is better current noise → 1MΩ is better)

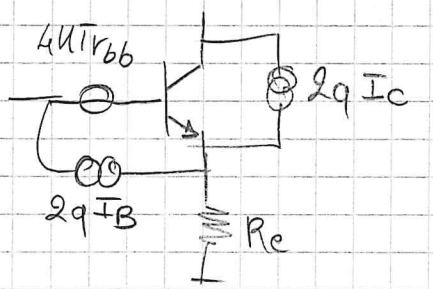
For CMOS:



High freq bound: poles of the sys → f_{MAX}
Low freq bound: observation time → f_{MIN}

Since integrated noise is $\log\left(\frac{f_{MAX}}{f_{MIN}}\right)$,
even though we have high observation time, very little power is integrated with a T_{OBS} increase

For bipolar:



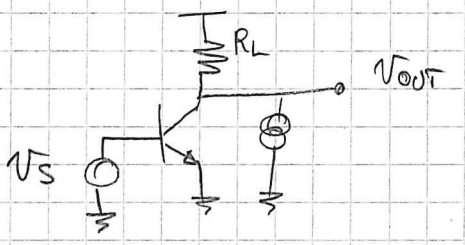
Base shot noise is very annoying:
- If $R_E \to \infty$, $2qI_C$ will recirculate (cascode)
- $2qI_B$ will always be present → stage will be noisy even with large degeneration (cascode BJTs are noisy, unlike CMOS)

bb: physical resistance between base and collector

Input referred noise

Consider just collector noise, what matters is SNR!

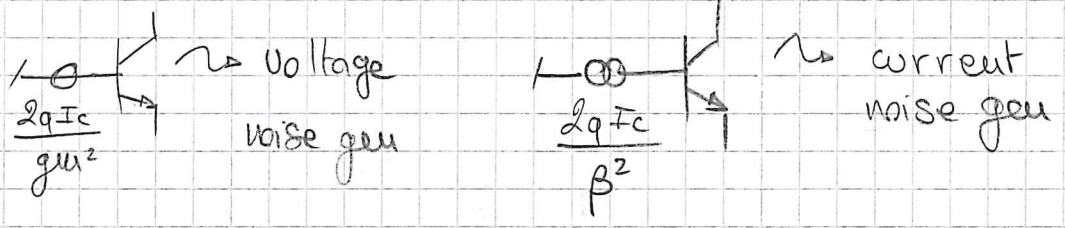
$$(SNR)^2 = \frac{\left[\int_0^{BW} |S_{signal}|^2 df\right] g_m^2 R_L^2}{2q I_C R_L^2 (BW)}$$



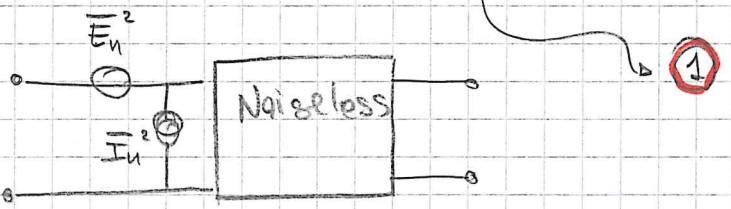
$$(SNR)^2 = \frac{\int_0^{BW} |S_{sig}|^2 df}{\frac{2q I_C}{g_m^2} BW}$$ → Comparing input voltage with input referred voltage noise!

$\frac{2q I_C}{g_m^2} BW \rightarrow \frac{2q}{I_C} V_{TH}^2 BW$ ↝ it's better to have large I_C to improve SNR

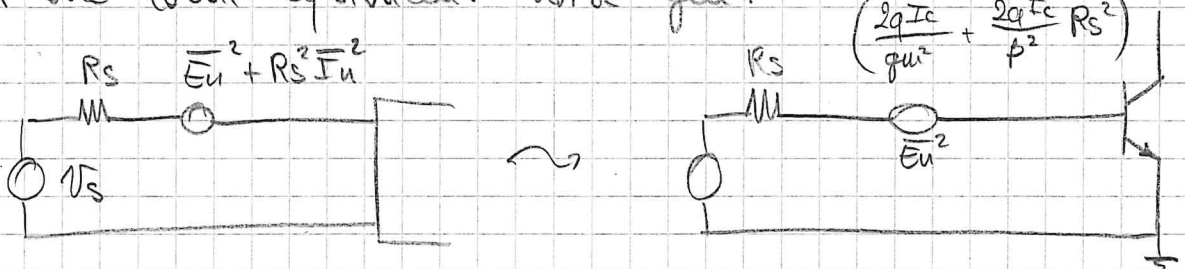
Input referred noise generators:



More in general, we model a noisy stage with a noiseless stage + two uncorrelated input noise generators:

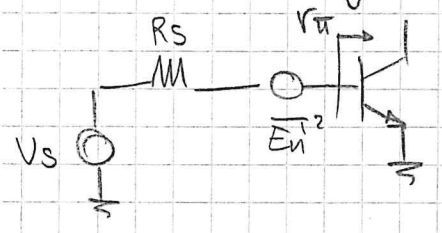


When we connect a thevenin eq input source, we can have just one total equivalent noise gen:



This is NOT correct because we did not take (1) into account!

By considering the full correlation, we need to:



$$\overline{E_n'}^2 \left(\frac{r_\pi}{R_s + r_\pi}\right)^2 g_m^2 = 2q I_c$$

full input referred noise

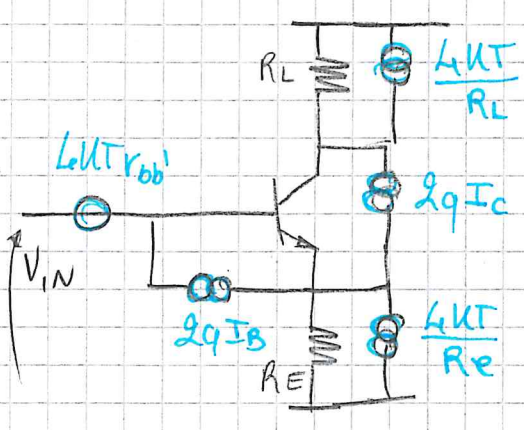
$$\overline{E_n}^2 = \frac{2qI_c}{g_m^2}\left(1 + \frac{R_s}{r_\pi}\right)^2 = \underbrace{\frac{2qI_c}{g_m^2}}_{\overline{E_n}^2} + \underbrace{\frac{2qI_c}{\beta^2} R_s^2}_{\overline{I_n}^2 \cdot R_s^2} + \underbrace{\frac{2qI_c}{g_m^2}\frac{2R_s}{r_\pi}}_{\text{double product (neglected before)}} \; (1)$$

Usually, because of ease of computation, we neglect (1),

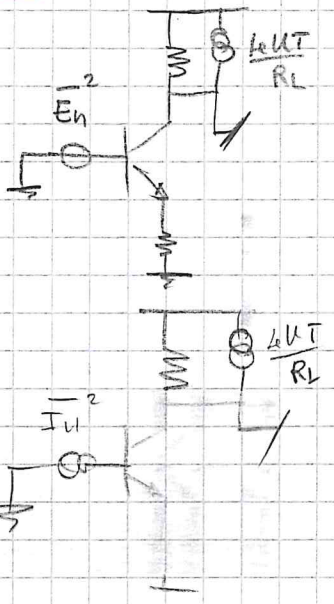
However, at very high frequency correlated sources become relevant so we will take (1) into account again

~~Bipolar analog stage input referred noise~~

4) Common emitter input referred noise



- load noise

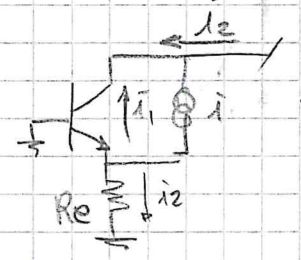


$$\overline{E_n}^2 \left(\frac{1}{\frac{1}{g_m}+Re}\right)^2 = \frac{4KT}{R_L} \rightarrow \overline{E_n}^2 = 4KT \frac{\left(\frac{1}{g_m}+Re\right)^2}{R_L}$$

$$\overline{I_n}^2 \beta^2 = \frac{4KT}{R_L} \rightarrow \overline{I_n}^2 = \frac{4KT}{\beta^2 R_L} \quad (1)$$

- BIT Ic shot noise

we neglect the base contribution $\frac{i_1}{\beta}$



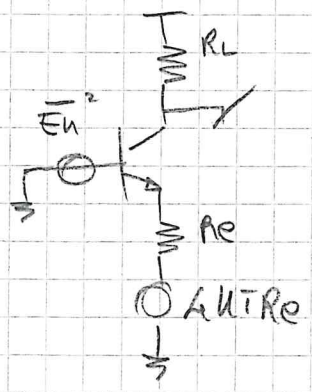
$$\rightsquigarrow i_2 \cong i \frac{1/g_m}{1/g_m + Re}$$

$$\overline{E_n}^2 \left(\frac{1}{\frac{1}{g_m}+Re}\right)^2 = 2qI_C \frac{1/g_m^2}{\left(\frac{1}{g_m}+Re\right)^2} \rightarrow \overline{E_n}^2 = \frac{2qI_C}{g_m^2}$$

It would be tempting to put $Re \rightarrow \infty$ to make $i_1 = i$, but this is not useful at all since gain would also be killed. In fact, to compute SNR we use $\overline{E_n}^2$ which does not have any Re dependance.

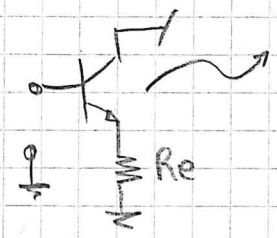
$\overline{I_n}^2 \beta^2 = 2qI_C \rightsquigarrow$ same as (1) $\rightarrow \overline{I_n}^2 = \frac{2qI_C}{\beta^2}$

- emitter resistor noise



$$\frac{4KTR_e}{\left(\frac{1}{g_m}+R_e\right)^2} \sim \frac{\overline{E_n}^2}{\left(\frac{1}{g_m}+R_e\right)^2}$$

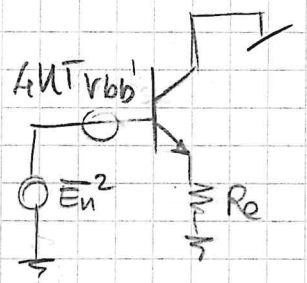
$$\overline{E_n}^2 = 4KTR_e$$



mosfet is OFF → no current noise

$$\overline{I_n}^2 = 0$$

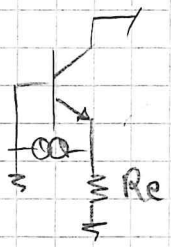
- $r_{BB'}$ resistor noise



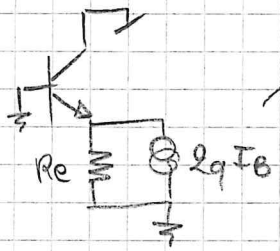
$$\overline{E_n}^2 = 4KTr_{BB'}$$

$$\overline{I_n}^2 = 0$$

- Base shot noise

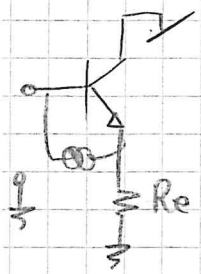


shift

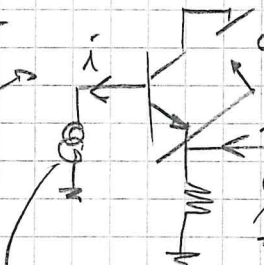


$$\overline{E_n}^2 = 2qI_BR_e^2$$

(based on previous results)

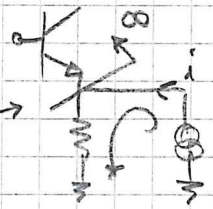


split



∞ because of the open generator

Negligible because →



$$\overline{I_n}^2 = 2qI_B$$

Total input equivalent noise

$$\overline{E_u}^2 = \frac{4KT}{R_L}\left(\frac{1}{g_m} + R_e\right)^2 + \frac{2qI_c}{g_m^2} + 4KTr_{bb'} + 2qI_B R_e^2 + 4KTR_e$$

$$\overline{I_u}^2 = \frac{4KT}{R_L}\cdot\frac{1}{\beta^2} + \frac{2qI_c}{\beta^2} + \cancel{0} + 2qI_B + \cancel{0}$$

R_L | I_c shot | $r_{bb'}$ | I_B shot | R_e

Note: by putting $R_e = 0$, $R_e \neq 0$ and by adjusting the gain (e.g. constant gain for both), we will see that feedback (i.e. degeneration of the emitter) will worsen the noise. On top of that, an active load will add even more noise.

Equivalent contributions w/o feedback ($R_e = 0$)

$$\overline{E_u}^2 = \underbrace{\frac{4KT}{R_L g_m^2}}_{①} + \underbrace{\frac{2qI_c}{g_m^2}}_{②} + \underbrace{4KTr_{bb'}}_{③}$$

Typically ② > ①: $2qI_c > \frac{4KT}{R_L}$ → $I_c R_L > 2V_{TH}$ → $V_{RL} > 2V_{TH}$

This is usually true because $V_{RL} \gg 50\,mV$ because of large gain so large R_L

What about ② vs ③?

$$\frac{2qI_c}{g_m^2} = \frac{2qI_c}{I_c}\cdot\frac{KT}{q}\cdot\frac{1}{g_m} = 2KT\frac{1}{g_m}$$ → called half noise in old literature

So we now compare $2KT\cdot\frac{1}{g_m}$ with $4KTr_{bb'}$ → $r_{bb'} \sim 100 \div 500\,\Omega$, $\frac{1}{g_m} \sim 25\,\Omega \div 2{,}5\,K\Omega$ (high bias ↑ / low bias ↑)

We clearly see that at low bias ③ is negligible with respect to ②, viceversa at high bias in which $4KTr_{bb'}$ is the ultimate noise limit:

$$\overline{E_u}^2 \simeq \frac{2qI_c}{g_m^2}$$ because we usually design amplifying stages at low bias (see question 1 on the β/I_c plot)

$$\overline{I_u^2} = \frac{4kT}{R_L}\cdot\frac{1}{\beta^2}\,①+\frac{2qI_C}{\beta^2}\,②+2qI_B\,③$$

Note: $\overline{I_u^2}$ is unchanged → feedback acts on voltage noise only.

Which source is dominant?

②

$$\frac{2qI_C}{\beta^2}=\frac{2qI_B}{\beta}\ll 2qI_B\ ③ \rightsquigarrow ② \text{ can be neglected}$$

$$\frac{4kT}{R_L\beta^2}\ll 2qI_B \longrightarrow \frac{2kT}{q}\cdot\frac{1}{\beta}\ll (I_B\cdot\beta)R_L \longrightarrow \frac{2V_{TH}}{\beta}\ll V_{R_L}\longrightarrow$$

Verify this ←

→ This relationship is always true so we verified ①≪③

Therefore $\overline{I_u^2}\simeq 2qI_B$

Dominant contributions with feedback ($R_E\neq 0$)

Remember that, in order to have good degeneration:

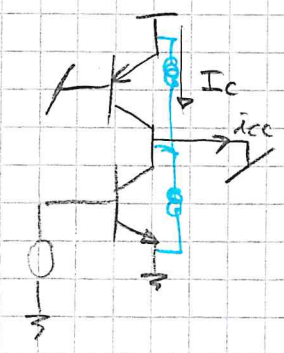
$g_m R_E \gg 1 \rightarrow V_{R_E}\gg V_{TH}$ or at least >1

For this reason $\frac{2qI_C}{g_m^2}=2kT\cdot\frac{1}{g_m}\ll 4kTR_E$

Therefore $\overline{E_u^2}\simeq 4kTR_E$ ⇝ feedback, in order to be good increases the overall noise

$\overline{I_u^2}$ remains unchanged because feedback does not affect it

5) Active load noise and other topologies



Note: we have two current generators back to back, we need to be careful not to push one of them into saturation because of mismatches

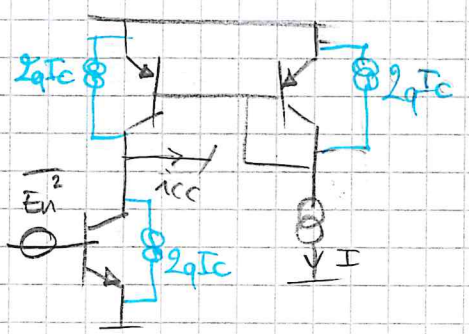
$$\overline{E_n^2} = 2 \cdot \frac{2qI_c}{g_m^2} + 4kTr_{bb'_{npn}} + 4kTr_{bb'_{pnp}} \left(\frac{g_{m_{pnp}}}{g_{m_{npn}}}\right)^2$$

$\rightarrow 1$

Usually negligible

Noise is doubled and we have no degrees of freedom since pnp and npn transistors share the same current, thus the same g_m.

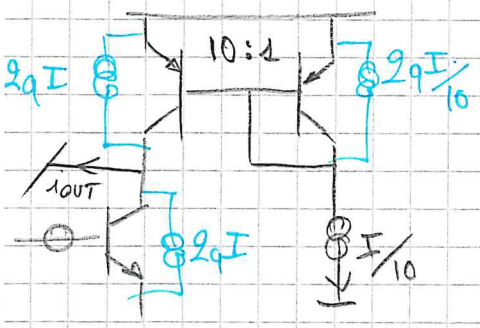
Mirror noise on an active load



Suppose g_m is the same for all BJTs:

$$\overline{E_n^2} = 3\,\overline{E_n^2}\Big|_{\text{single generator}}$$

Of course, we usually change the mirror ratio not to waste too much power:



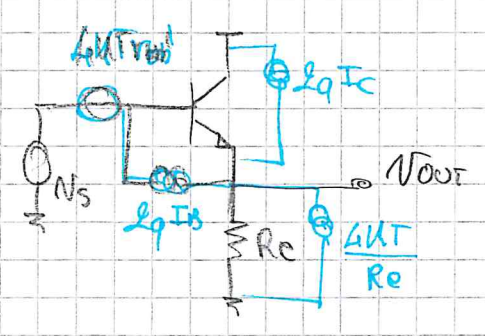
→ Reduced I_c by 10 → noise lowers by 10. Great news! Nope;

$$i_n\Big|_{out} = 2 \cdot 2qI_c + 2q\frac{I_c}{10} \cdot (10)^2$$

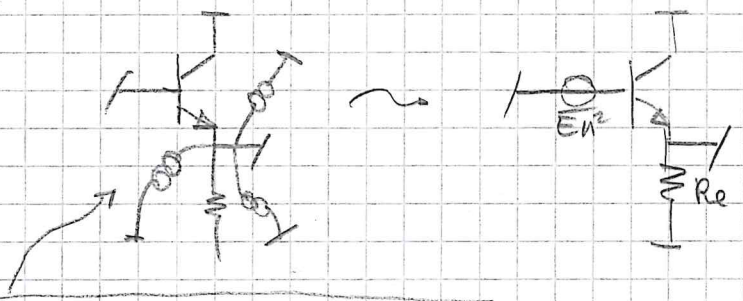
At the end of the day power is lowered but noise is 10 times more!

We cannot beat thermodynamics, tradeoffs between power and noise will always be there

Emitter follower noise



It's clear that when we short Vout, all current generators are in parallel:



$$\overline{E_n^2} = 4KTr_{bb'} + \frac{2qI_B}{g_m^2} + \frac{2qI_C}{g_m^2} + \frac{4KT}{R_e}\cdot\frac{1}{g_m^2}$$

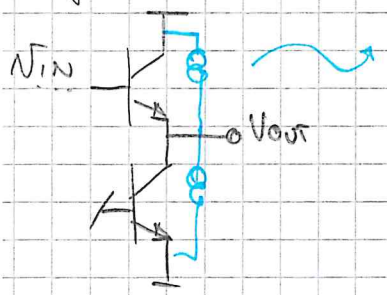
→ Trivial computation

$$\overline{I_n^2} = \cancel{} + 2qI_B + \frac{2qI_C}{\beta^2} + \frac{4KT}{R_e}\cdot\frac{1}{\beta^2}$$

to be verified

Typically $\frac{2qI_C}{g_m^2} \gg \frac{4KT}{R_e g_m^2}$ → $I_C R_e \gg 2V_{TH}$ typically true

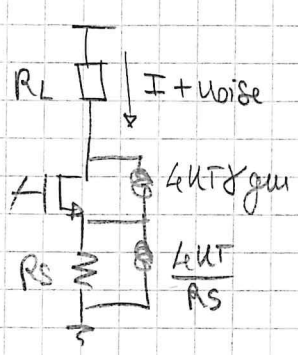
The best emitter follower has a current generator as degeneration:

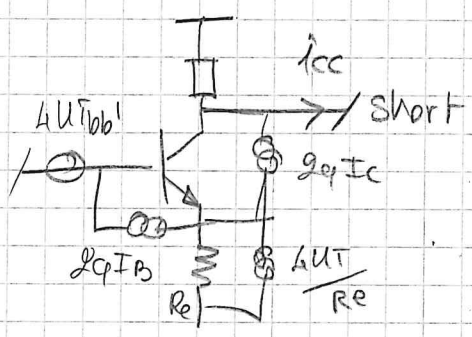


In the best case scenario, we double the noise.

Noise in bipolar current generators

A degenerated MOS stage has (in theory) no noise limit, while BJTs do have:





$$i_{noise_{OUT}}\Big|_{short} = 2qI_C\left(\frac{\frac{1}{g_m}}{\frac{1}{g_m}+R_e}\right)^2 + \frac{4kT}{R_e}\left(\frac{R_e}{R_e+\frac{1}{g_m}}\right)^2 + 4kTr_{bb'}\frac{1}{\left(\frac{1}{g_m}+R_e\right)^2} + 2qI_B\left(\frac{R_e}{R_e+\frac{1}{g_m}}\right)^2$$

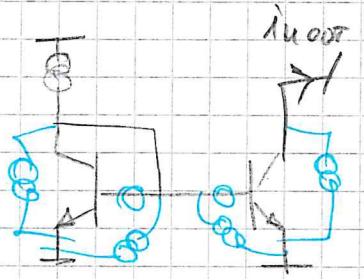
(the second factor $\to 1$; the last factor $\to 1$)

If $R_e \to \infty$ we can see that $2qI_B$ will be the upper limit

verify that $2qI_B > \frac{4kT}{R_e}$ $\longrightarrow$ $I_C R_e > 2\beta V_{TH}$ $\longrightarrow$

$\longrightarrow$ very difficult to achieve since $2\beta V_{TH} \sim 5 \div 10\,V$

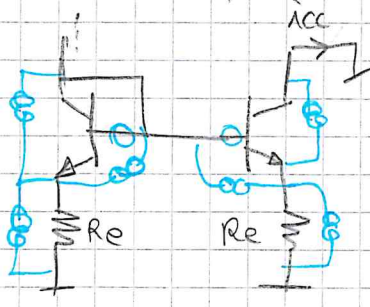
Current mirrors noise



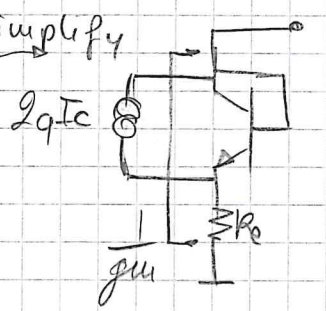
$$i_{NOUT} = 2\cdot 2qI_C + 2\cdot 2qI_B + 2\cdot 4kTr_{bb'}g_m^2\left(\frac{\beta}{\beta+1}\right)^2$$

($\to 1$)

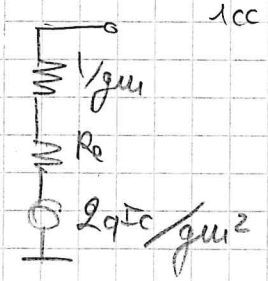
We could also have a degenerated mirror. It is not common, but it is usually done to increase the impedance and linearity:



Simplify

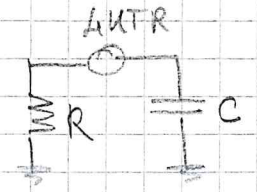


=



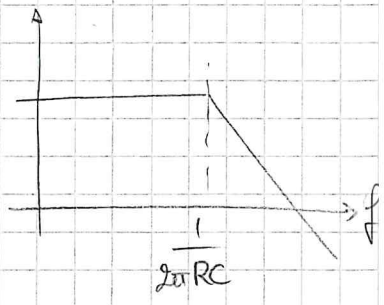
$$i_{cc} = 2\cdot 2qI_C\left(\frac{1/g_m}{\frac{1}{g_m}+R_e}\right)^2$$

6) Sampled noise

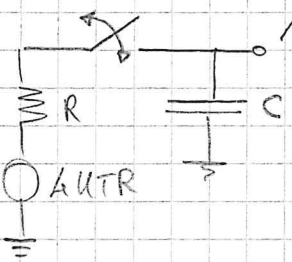


C can be intentional or parasitic

$$\sigma_V^2 = \frac{4KTR}{4RC} \approx \frac{KT}{C}$$

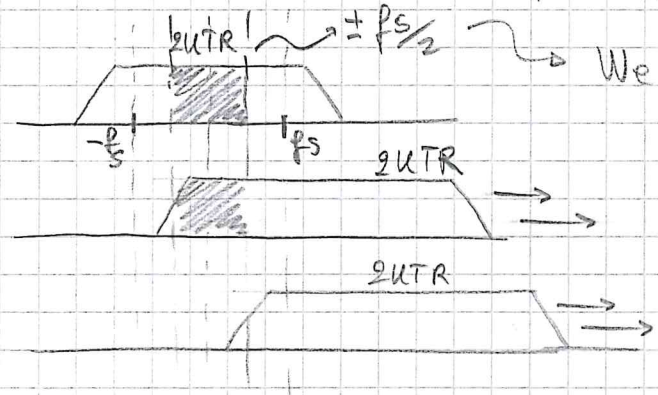


Sampled sys:



→ When we "freeze" the voltage on C, we also freeze the noise value → $\sigma_V^2 = \frac{KT}{C}$

Keep in mind spectrum folding:



→ We integrate noise over a fs bandwidth

The area of this will be

$$\overline{\sigma_V}^2 = KT/C$$

This changes with oversampling, since we're spreading the noise on a larger bandwidth compared to the signal one:

Note that:

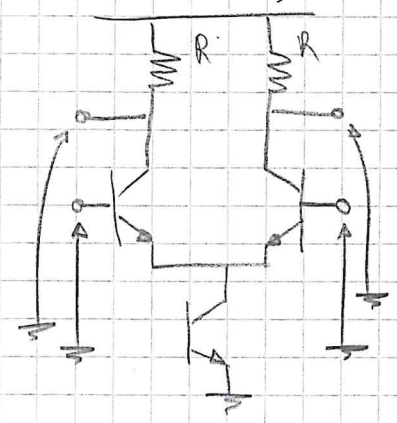
- If we increase fs to reduce the noise, it means that we need to reduce the capacitance values → higher noise!

e.g: $fs' = 10\,fs \rightarrow C' = C/10 \rightarrow \text{noise}|_{C'} = 10 \cdot \text{noise}|_{C}$ → zero advantage

Oversampling works best with quantization noise.

- If we increased fs but keeping the capacitances the same, we would need to burn more power because of the higher requirement on speed with a large capacitive load → power/noise tradeoff is always there

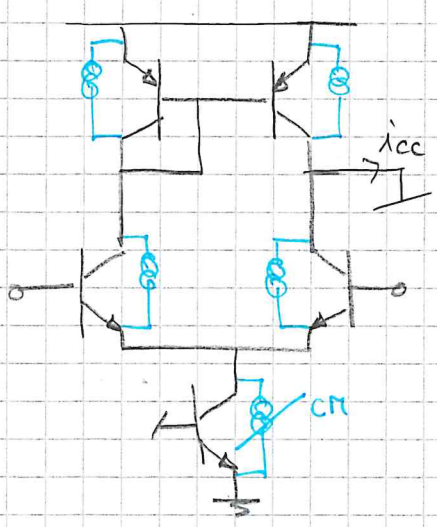
7) Differential pair noise



We have two IN, two OUT. It means that we can apply the differential mode and common mode, which "should" be orthogonal (that's why they're called modes).
We will take into account $\overline{E_n^2}$ only when input referring, because the input noise equivalence for the input noise current generator does not always work, while it's well justified for $\overline{E_n^2}$.

Note:

if $R_1 \neq R_2$ ⇝ Stage is unbalanced, thus the tail noise generator in will reach the output even though it should given a CM contribution only.
That is why it is always best to compute the "final" SNR @ OUT instead of input referring everything.



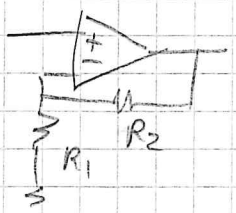
$$i_{OUT}\big|_{TOT} = 4 \cdot 2qI_C$$

$$\overline{E_n^2}\, g_m^2 = 2qI_C \cdot 4 \longrightarrow \overline{E_n^2} = \frac{4 \cdot 2qI_C}{g_m^2}$$

Note: in bipolar, if we don't use passive loads, active load noise is as important as the input pair

8) Offset: matching issues

High performance systems can be built with high accuracy even though integrated components can have up to 20% tolerance. How come? We design everything relying on the ratio between components and not on the absolute values. e.g.:



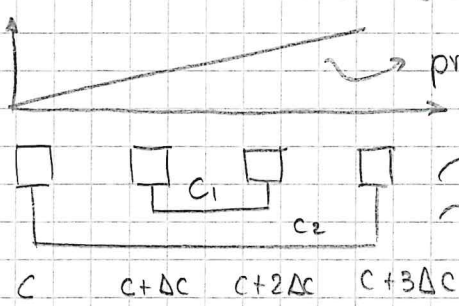
$\left(\frac{R_2}{R_1}+1\right) = G$, suppose $R_2 = R_2 + \Delta R_2$

$R_1 = R_1 + \Delta R_1$

$$\frac{R_2+\Delta R_2}{R_1+\Delta R_1} = \frac{R_2}{R_1}\cdot\frac{1+\frac{\Delta R_2}{R_2}}{1+\frac{\Delta R_1}{R_1}} \overset{\text{small error}}{\approx} \frac{R_2}{R_1}\left(1+\frac{\Delta R_2}{R_2}\right)\left(1-\frac{\Delta R_1}{R_1}\right) \overset{\text{neglect 2nd order product}}{\approx}$$

$$\approx \frac{R_2}{R_1}\left(1-\frac{\Delta R_1}{R_1}-\frac{\Delta R_2}{R_2}\right)$$ ⇝ We always have a relative error that's why we can achieve good tolerances

Consider two capacitors $C_1 = C_2 = C$, we can use the common centroid technique to cancel any process gradient:



$C_2 = C + \Delta C + C + \Delta C = 2C + 3\Delta C$

$C_1 = C + C + 3\Delta C = 2C + 3\Delta C$

⇝ capacitors are insensitive to gradient

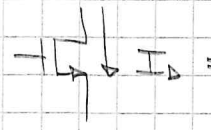
What's left now is just random fluctuations. Pelgrom formula states that

$\frac{\sigma_{\Delta C}}{C} \propto \frac{1}{\sqrt{WL}}$ ⇝ The larger the area, the smaller the variance

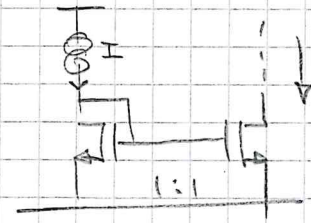
Therefore $\frac{C_1}{C_2} \approx \frac{C_1}{C_2}\left[1+\frac{\Delta C_1}{C_1}+\frac{\Delta C_2}{C_2}\right]$ ⇝ They improve given a larger area (of course ratio C_1/C_2 is the same)

SW. capacitor filters are particularly helpful because they do not rely on RC or $\frac{C}{gm}$ constants but on capacitors <u>ratio</u>!

Current generator mismatches



$I_D = K (V_{GS} - V_T)^2$ → Usually K, V_T have variance



Assume a small error:

$$dI = dK (V_{GS} - V_T)^2 - 2K (V_{GS} - V_T) dV_T$$

$$\frac{dI}{I} = \frac{dK}{K} - \frac{2\,dV_T}{V_{OV}} = \frac{dK}{K} - \frac{g_m}{I} dV_T$$

If we repeat the measurement on 90 samples, we'll see:

$$\sigma_{\frac{\Delta I}{I}}^2 = \sigma_{\frac{\Delta K}{K}}^2 + \sigma_{V_T}^2 \frac{4}{(V_{GS} - V_T)^2}$$

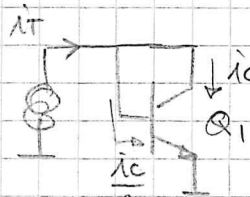
→ This assumes $\Delta V_T, \Delta K$ to be uncorrelated → not true

$\frac{\Delta K}{K}$ → adimensional; V_T → $[V^2]$

Typically, since we work with small $V_{OV} = V_{GS} - V_T$, the $\sigma_{V_T} \frac{4}{V_{OV}^2}$ factor is more dominant

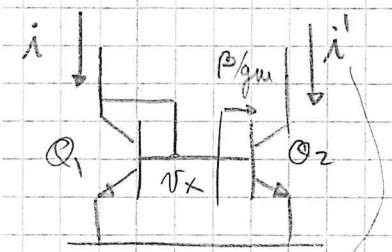
$$\sigma_{\frac{\Delta I}{I}}^2 = \frac{A_K^2}{WL} + \frac{A_{V_T}^2}{WL} \cdot \frac{4}{V_{OV}^2}$$

BJT mirror mismatch (next page uses different computation for V_{BE})



$$i_T = i_C + \frac{i_C}{\beta} = i_C \left(\frac{\beta+1}{\beta}\right) \qquad V_T = \frac{i_C}{g_m} = \frac{i_T}{g_m} \cdot \frac{\beta}{\beta+1}$$

$$Req_1 = \frac{V_T}{i_T} = \frac{\beta}{\beta+1} \cdot \frac{1}{g_m}$$



$$V_x = i \cdot (Req_1 // Req_2) = i \frac{\frac{\beta}{\beta+1} \cdot \frac{1}{g_m} \cdot \frac{\beta}{g_m}}{\frac{\beta}{\beta+1} \cdot \frac{1}{g_m} + \frac{\beta}{g_m}} = i \cdot \frac{1}{g_m} \cdot \frac{\frac{\beta}{\beta+1}}{\frac{\beta+2}{\beta+1}}$$

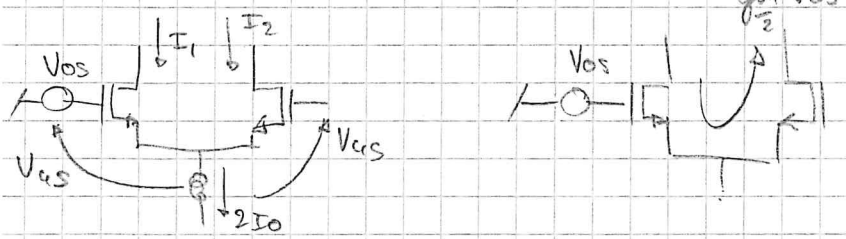
$$= i \frac{\beta}{g_m} \cdot \frac{1}{\beta+2}$$

$$i' = g_m V_x = \frac{\beta}{\beta+2}$$

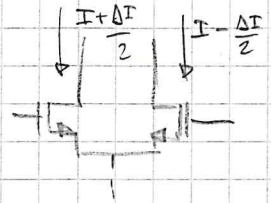
This is very stupid, but it uses voltages and currents to get to the same result

Offset of a differential pair

MOSFET



- V_T mismatch is modeled as a ΔV_T generator on one of the two MOS → it is directly comparable with V_{OS}
- K mismatch will introduce a $I_2 - I_1 = \Delta I$ modeled as:



$$\frac{g_m}{2} V_{OS} = \frac{\Delta I}{2} \rightarrow V_{OS} = \frac{\Delta I}{g_m} = \frac{\Delta I}{I} \frac{V_{OV}}{2} = \frac{\Delta K}{K} \frac{V_{OV}}{2}$$

$I \propto K$

If ΔV_T, ΔK are uncorrelated (not true)

$$\sigma_{OS}^2 = \sigma_{V_T}^2 + \sigma_{\frac{\Delta K}{K}}^2 \frac{V_{OV}}{4}$$

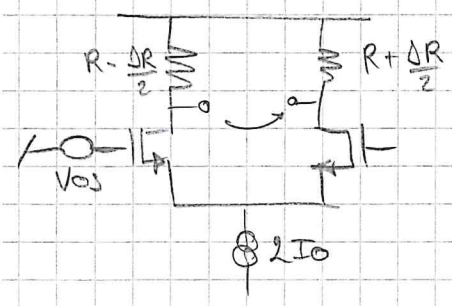
Note that noise / offset calculations are the same and most of the times if noise is high, then also offset will be relatively high.

e.g.: consider the input equivalent noise of a MOS diff pair

$$\overline{E_n}^2 = \frac{(4kT\gamma g_{mn} + 4kT\gamma g_{mp}) \cdot 2}{g_{mn}^2} = 8kT\gamma \left[\frac{1}{g_{mn}} + \frac{g_{mp}}{g_{mn}^2} \right]$$

While $\sigma_{V_{OS}}^2 = \sigma_{V_{Tn}}^2 + \sigma_{V_{Tp}}^2 \left(\frac{g_{mp}}{g_{mn}} \right)^2$ similarities are shared

Same offset reasoning can be done with passive loads:

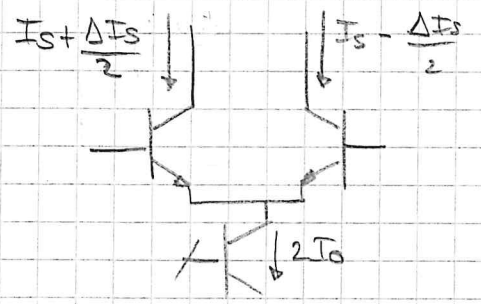


$$g_m V_{OS} \cdot R = \Delta R \cdot I_D$$

$$V_{OS} = \frac{I_D}{g_m} \left(\frac{\Delta R}{R} \right) = \frac{\Delta R}{R} \cdot \frac{V_{OV}}{2}$$

$$\sigma_{OS}^2 \Big|_R = \sigma_{\frac{\Delta R}{R}}^2 \cdot \frac{V_{OV}^2}{4}$$

BJT differential pair offset



For bipolar transistors:
- emitter area mismatch
- base doping mismatch

$I_C = I_S e^{V_{BE}/V_{TH}}$

A_E = emitter area

$$g_m \frac{V_{OS}}{2} = \frac{\Delta I}{2} \rightarrow V_{OS} = \frac{\Delta I}{g_m} = \frac{\Delta I}{I} \cdot V_{TH} = \frac{\Delta I_S}{I_S} \cdot V_{TH} \quad (1)$$

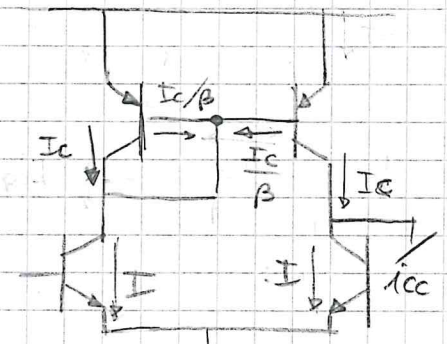
($I_C \propto I_S$)

We sometimes find $\frac{\Delta I_S}{I_S}$ expressed through pelgrom $\sigma^2\frac{\Delta I_S}{I_S} = \frac{A_{\Delta I_S}}{A_E}$

(1) We have V_{TH} instead of V_{OV} (MOS), since $V_{TH} < V_{OV}$

offset is usually lower for BJTs compared to MOSFETs.

BJT systematic offset of the current mirror



$V_{BE3} = V_{BE4} \Rightarrow V_{TH} \ln\left(\frac{I_{C3}}{I_{S3}}\right) = V_{TH} \ln\left(\frac{I_{C4}}{I_{S4}}\right)$

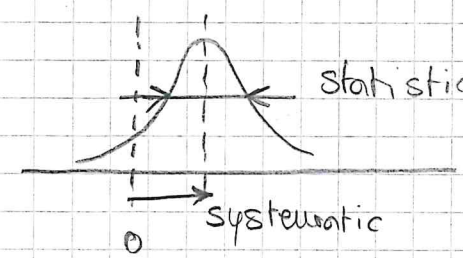
if $I_{S3} = I_{S4}$ then $I_{C3} = I_{C4} = I_C$

$$I = I_C + \frac{I_C}{\beta} + \frac{I_C}{\beta} = I_C\left(\frac{\beta+2}{\beta}\right) \rightarrow I_C = I\left(\frac{\beta}{\beta+2}\right)$$

If diff pair has perfect balance I, a small fraction will flow to 2nd stage thus generating a systematic offset ($i_{CC} = I_C - I$)

$$V_{OS} \cdot \frac{g_m}{2} \cdot 2 = I \cdot \frac{2}{\beta+2} \rightarrow V_{OS} = \frac{I}{g_m} \cdot \frac{2}{\beta} = \frac{2V_{TH}}{\beta}$$

($\frac{2}{\beta+2} \rightarrow$ Neglect)



- because $I_{CC} = I - I_C = I_0\left(1 - \frac{\beta}{\beta+2}\right) = I_0\frac{\beta}{\beta+2}$

Remember that this needs to be balanced by design since it's deterministic.

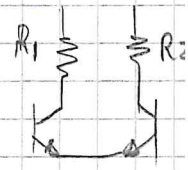
For MOSFET sys. offset recall the analog circuit design notes

Large relative error offset

We said that, for a small error:

$$V_{OS}\Big|_{I_S} = V_{TH}\frac{\Delta I_S}{I_S} \quad (1)$$ and we can easily find $$V_{OS}\Big|_{R} = V_{TH}\frac{\Delta R}{R} \quad (2)$$ (passive load)

What about a large error?



$$V_{OS} = V_{BE1} - V_{BE2} = V_{TH}\ln\left(\frac{I_{C1}}{I_{S1}}\right) - V_{TH}\ln\left(\frac{I_{C2}}{I_{S2}}\right) = V_{TH}\ln\left(\frac{I_{C1}}{I_{C2}}\cdot\frac{I_{S2}}{I_{S1}}\right)$$

To have $V_{OUT\,diff} = 0$ (no sys. offset) $I_{C1}R_1 = I_{C2}R_2$ $\frac{I_{C1}}{I_{C2}} = \frac{R_2}{R_1}$

$$V_{OS} = V_{TH}\ln\left(\frac{R_2}{R_1}\frac{I_{S2}}{I_{S1}}\right) = V_{TH}\ln\left[\frac{R-\frac{\Delta R}{2}}{R+\frac{\Delta R}{2}}\cdot\frac{I_S-\frac{\Delta I_S}{2}}{I_S+\frac{\Delta I_S}{2}}\right]$$

$$= V_{TH}\ln\left[\frac{1-\frac{\Delta R}{2R}}{1+\frac{\Delta R}{2R}}\cdot\frac{1-\frac{\Delta I_S}{I_S}}{1+\frac{\Delta I_S}{I_S}}\right]$$ ↝ we stop here for large errors

Assume now ΔR, ΔI_S small → let us find again (1) and (2):

$\frac{1}{1+x} \simeq 1-x$ for $x \to 0$ so

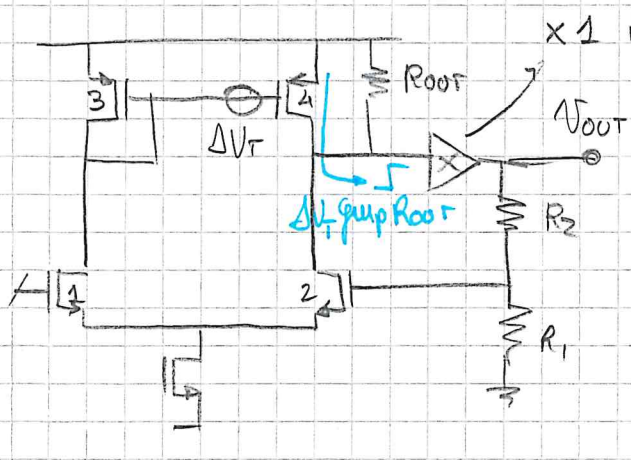
$$V_{OS} \simeq V_{TH}\ln\left[\left(1-\frac{\Delta R}{2R}\right)^2\right] + V_{TH}\ln\left[\left(1-\frac{\Delta I_S}{2I_S}\right)^2\right] = 2V_{TH}\left[\ln\left(1-\frac{\Delta R}{2R}\right) + \ln\left(1-\frac{\Delta I_S}{2I_S}\right)\right]$$

$\ln(1+x) \simeq x$ for $x \ll 1$

$$V_{OS} \simeq -2V_{TH}\frac{\Delta R}{2R} - 2V_{TH}\frac{\Delta I_S}{I_S} \simeq V_{TH}\frac{\Delta R}{R} + V_{TH}\frac{\Delta I_S}{I_S}$$

↳ (2) ↳ (1)

Offset + feedback



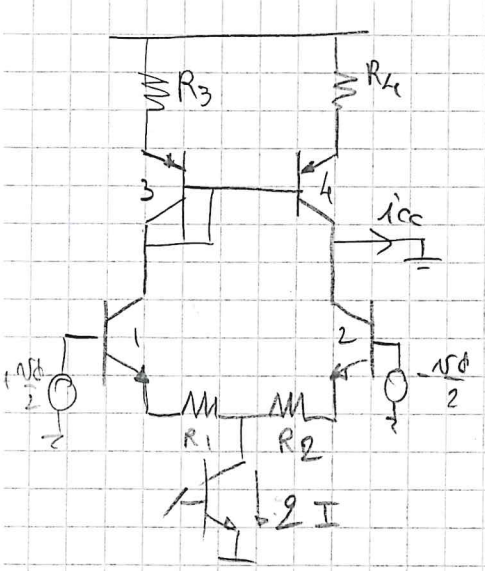
Consider a ΔV_T mismatch on M_4, we would see a $g_{mp}\Delta V_T R_{OUT}$ step at V_{OUT} without feedback, let's see what happens instead

$$G_{loop} = -g_{mn} \cdot R_{OUT}\left(\frac{R_1}{R_1+R_2}\right)$$

$$V_{OUT} = \frac{\Delta V_T\, g_{mp} R_{OUT}}{1 + g_{mn} R_{OUT}\left(\frac{R_1}{R_1+R_2}\right)} \overset{R_{OUT}\to\infty,\ G_{loop}\to\infty}{=} \Delta V_T \frac{g_{mp}}{g_{mn}}\left(1+\frac{R_2}{R_1}\right)$$

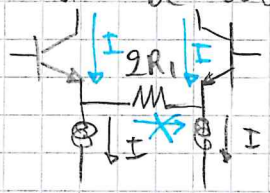
Feedback unbalances the stage on M_2 so that the offset is reduce at the output.
In principle, we should consider the common mode as well but here we consider CMRR $\to\infty$. It's the same thing we do for $\overline{E_n^2}$ so even more similarities between noise/offset. We consider ∞ CMRR because offset is usually more relevant just for differential mode

10) Exam example on degenerated mirror + degenerated input pair noise and offset

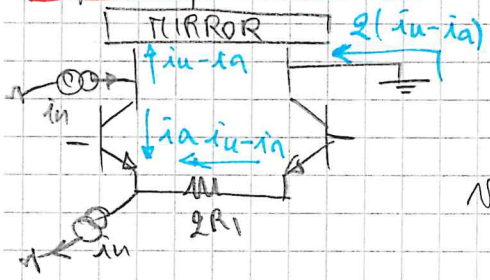


$$i_{cc}|_{OUT} = \frac{v_d}{\frac{2}{g_m} + 2R_1} \qquad r_o = \infty \quad \beta = \infty$$

Pros/cons of degeneration

+ $R_{3,4}$ increase mirror impedance (for finite r_o)
+ $R_{1,2}$ = input = r_π
+ input degeneration has a smaller g_m → SR ✓
(smaller g_m but with the same 2I g_m)
− R_1, R_2, R_3, R_4 introduce noise + mismatch
− larger voltage headroom needed because of R_1, R_2 bias.
It can be improved with  but the two new generators will add noise and mismatches since they are not CM any more

Input pair noise:



$$2(i_u - i_n) = 2 \cdot i_u \frac{1/g_{m12}}{\frac{2}{g_{m12}} + 2R_{12}} = i_{cc}$$

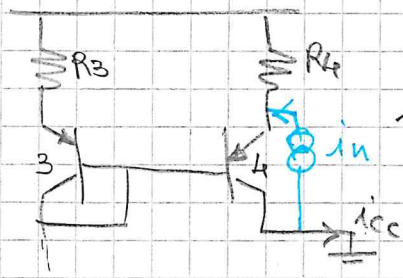
$$v_{n\,input} \cdot \frac{1}{\frac{2}{g_{m12}} + 2R_{12}} \cdot 2 = i_{cc}$$

→ 2 transistors

$$\rightarrow \overline{v_{noise}|_{IN}^2} = \frac{\overline{i_u^2}}{g_{m12}^2} \rightarrow \overline{E_u^2}\Big|_{\substack{in\\pair}} = 2 \cdot \frac{2qI_c}{g_{m12}^2}$$

Note: degeneration, as always, does not improve noise (feedback almost always does not improve noise!)

Mirror transistors noise Q_4



$$i_{cc} = i_n \cdot \frac{1/g_{m3,4}}{R_{3,4} + 1/g_{m3,4}} = \frac{v_n|_{IN}}{\frac{2}{g_{m1,2}} + 2R_1} \cdot 2$$

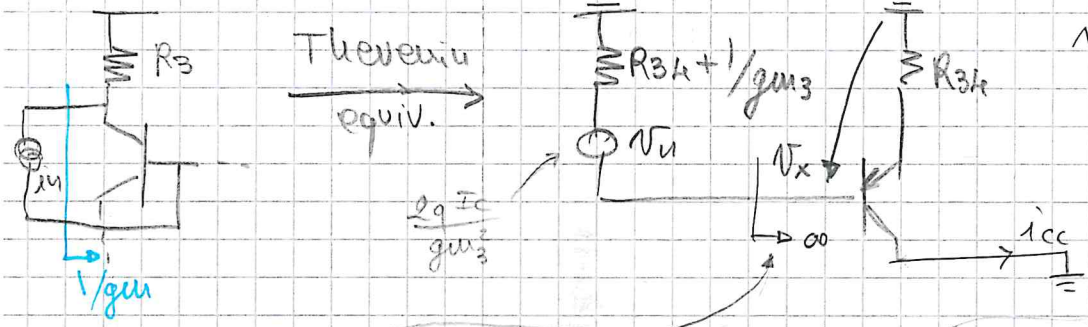
$$v_n|_{IN} = \frac{i_n}{g_m}\left(\frac{1 + g_m R_{12}}{1 + g_m R_{34}}\right)$$

→ bipolar must have same g_m because of the same current

$$\overline{E_n^2}\Big|_{Q_4} = \frac{2qI_C}{g_m^2}\left(\frac{1 + g_m R_{12}}{1 + g_m R_{34}}\right)^2$$

→ Degeneration of the input pair increases the noise of the other stages because of the lower differential gain

Mirror transistor noise Q_3



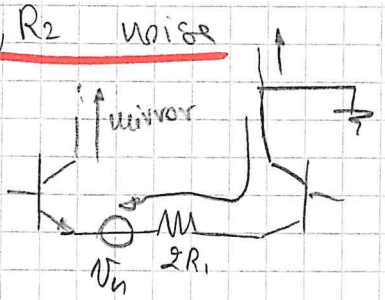
Since $\beta \to \infty$ $\quad v_x \approx v_n \rightarrow i_{cc} = v_x \cdot \frac{1}{\frac{1}{g_{m4}} + R_{3,4}} \rightarrow$

$$\rightarrow \overline{i_{cc}^2} = \frac{2qI_C}{g_m^2} \cdot \left(\frac{1}{\frac{1}{g_m} + R_{3,4}}\right)^2$$

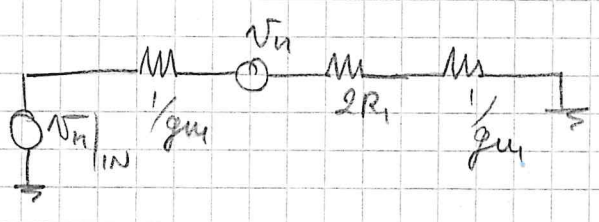
→ exactly like Q_4 noise →

$$\overline{E_n^2}\Big|_{Q_3} = \overline{E_n^2}\Big|_{Q_4}$$

R_1, R_2 noise



small signal equivalence →

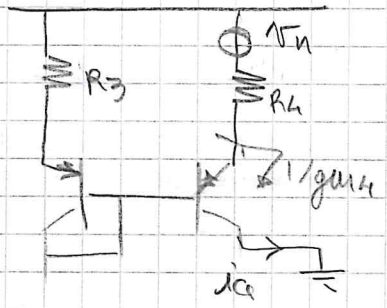


$\sqrt{v_n}|_{IN}$ and $\sqrt{v_n}$ are on the same loop,

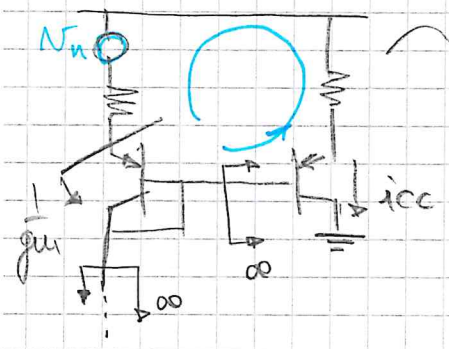
therefore → $\overline{E_n}|^2_{R_{12}} = 4KT(2R_1)$

Note: R_1, R_2 increase Q_3, Q_4 noise and their noise is directly comparable to the input differential pair noise → their contribution (remember that $g_m R_e \gg 1$) will most probably be the largest one.

R_3, R_4 noise



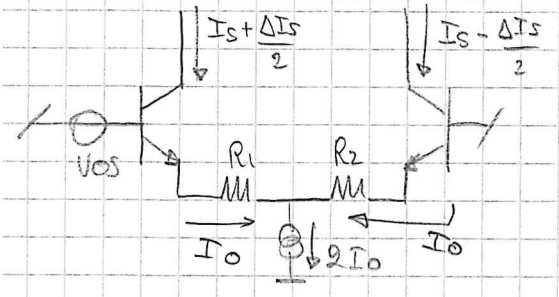
$$i_{cc} = \frac{\sqrt{v_{n4}}}{\frac{1}{g_{m4}} + R_4} \quad (\sqrt{v_{n4}} \text{ from } 4KTR_{34}) \longrightarrow \overline{E_n^2}|_{R_4} = 4KTR_{34}\left(\frac{1+g_m R_{12}}{1+g_m R_{34}}\right)^2$$



Since we're on the same loop, we can easily move the generator from left to right so that

$$\overline{E_n^2}|_{R_3} = \overline{E_n^2}|_{R_4}$$

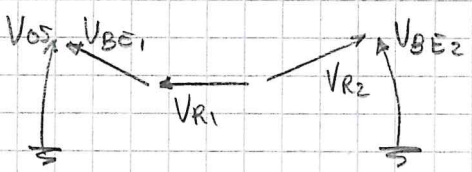
Input pair offset



$R_1 = R_2$

We place V_{OS} in order to balance the output current to ~~0~~. ($I_{Q_1} = I_{Q_2} = I_0$)

Since $V_{R_1} = V_{R_2}$ (trivial), $V_{BE_1} \neq V_{BE_2}$:

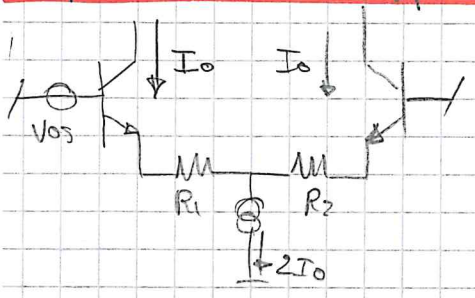


$$V_{OS} = V_{BE_1} + \cancel{I_0 R_1} - \cancel{I_0 R_1} - V_{BE_2}$$

$$= V_{BE_1} - V_{BE_2} \overset{\sim}{=} -V_{TH}\frac{\Delta I_S}{I_S}$$

small error (refer to offset theory)

Input resistor offset



$R_1 = R_1 + \Delta R_1/2$

$R_2 = R_1 + \Delta R_1/2$

By balancing using V_{OS}, we have $V_{BE_1} = V_{BE_2}$, so

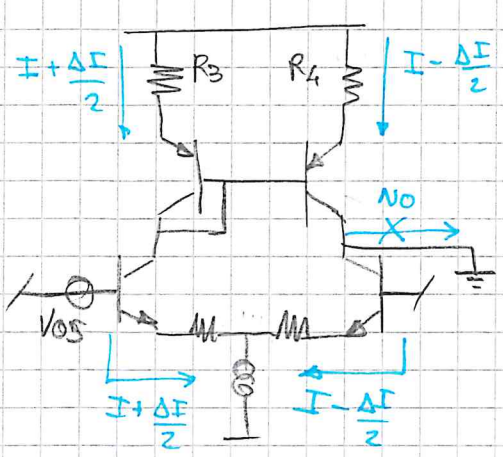
$$V_{OS} = \cancel{V_{BE_1}} + I_0\left(R_1 + \frac{\Delta R_1}{2}\right) - I_0\left(R_1 - \frac{\Delta R_1}{2}\right) - \cancel{V_{BE_2}} = (I_0 R_1)\frac{\Delta R_1}{R_1}$$

$I_0 R_2 \sim 1V$ → Voltage headroom on bias

$\Delta R_1/R_1$ ~ is usually small

Note: R_1, R_2 do not have any effect on other offset contribution and moreover they add themself a significant one!

R_3, R_4 offset



$$R_3 = R_3 + \Delta R/2$$

$$R_4 = R_3 - \Delta R/2$$

$I_{Q_3} \neq I_{Q_4} \rightarrow V_{BE_3} \neq V_{BE_4}$

V_{OS} unbalances the input pair so that $i_{OUT} = 0$ and $i_{DIFF}\big|_{V_{OS}} = \Delta I$

$$\Delta I = \frac{V_{OS}}{\frac{2}{g_{m_{12}}} + 2R_{12}} \cdot 2 \qquad (2)$$

Now we need to link ΔI to ΔR:

$$\left(R_3 + \frac{\Delta R_3}{2}\right)\left(I + \frac{\Delta I}{2}\right) + V_{TH} \ln\left(\frac{I+\frac{\Delta I}{2}}{I_S}\right) = \left(R_3 - \frac{\Delta R_3}{2}\right)\left(I - \frac{\Delta I}{2}\right) + V_{TH} \ln\left(\frac{I-\frac{\Delta I}{2}}{I_S}\right)$$

$$R_3(\Delta I) + \Delta R_3 I + V_{TH} \ln\left(\frac{1+\frac{\Delta I}{2I}}{1-\frac{\Delta I}{2I}}\right) = 0$$

$\frac{1}{1-x} \sim 1+x$ for small x

$\ln(1+x) \sim x$ if $x \ll 1$

$$R_3 \Delta I + \Delta R_3 I + 2V_{TH} \ln\left(1+\frac{\Delta I}{2I}\right) \approx R_3 \Delta I + \Delta R_3 I + \frac{V_{TH}}{I} \cdot \Delta I$$

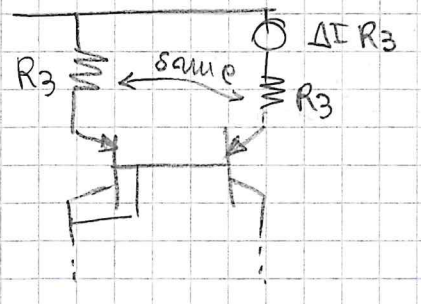
($\frac{V_{TH}}{I} = 1/g_m$)

$$\Delta I = \frac{-I}{R_3 + \frac{1}{g_m}} \Delta R_3 \qquad (1)$$

We plug (1) into (2) $\rightarrow$ $V_{OS} = -I \Delta R_3 \dfrac{1 + g_{m_{12}} R_{12}}{1 + g_{m_{34}} R_{34}}$

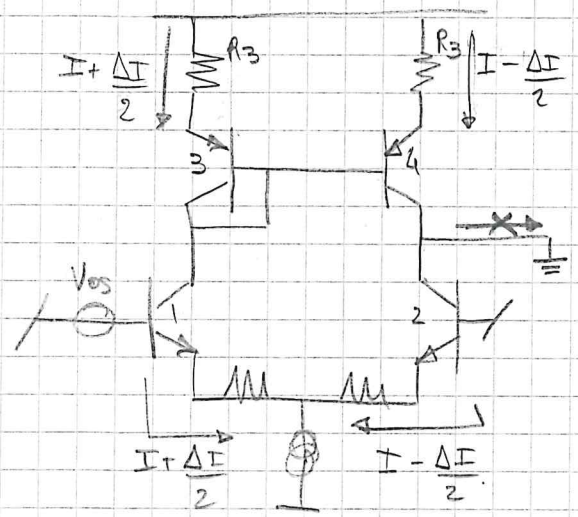
We find noise similarities again!

We can alternatively see this as:



$\Delta I R_3$ ~ unbalancing voltage generator $\rightarrow$ this leads to reason exactly like what we did for R_{34} noise

Mirror generator offset



Since $I_C \propto I_S \rightarrow \Delta I_S \rightarrow \Delta I_C$!

So $V_{R_3} + V_{BE_3} = V_{R_4} + V_{BE_4}$

$$R_3\left(I+\frac{\Delta I}{2}\right) + V_{TH}\ln\left(\frac{I+\frac{\Delta I}{2}}{I_S+\frac{\Delta I_S}{2}}\right) = R_3\left(I-\frac{\Delta I}{2}\right) + V_{TH}\ln\left(\frac{I-\frac{\Delta I}{2}}{I_S-\frac{\Delta I_S}{2}}\right)$$

$$R_3\,\Delta I = -V_{TH}\ln\left[\left(\frac{1+\frac{\Delta I}{2I}}{1+\frac{\Delta I_S}{2I_S}}\right)\frac{I}{I_S}\cdot\left(\frac{1-\frac{\Delta I_S}{2I_S}}{1-\frac{\Delta I}{2I}}\right)\frac{I_S}{I}\right] \cong -V_{TH}\ln\left(\left(1+\frac{\Delta I}{2I}\right)^2\left(1-\frac{\Delta I_S}{2I_S}\right)^2\right)$$

$\frac{1}{1-x} \sim x+1$

$$R_3\,\Delta I \cong -2V_{TH}\ln\left(1+\frac{\Delta I}{2I}\right) - 2V_{TH}\ln\left(1-\frac{\Delta I_S}{2I_S}\right) \cong$$

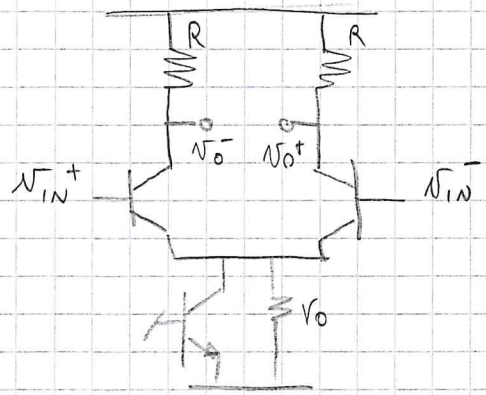
$$R_3\,\Delta I \cong V_{TH}\frac{\Delta I}{I} - V_{TH}\frac{\Delta I_S}{I_S} \longrightarrow \Delta I = \frac{V_{TH}\frac{\Delta I_S}{I_S}}{R_3 + 1/g_{m_{34}}}$$

$$V_{OS}\,\frac{1}{\frac{2}{g_m}+2R_1}\cdot 2 = \Delta I = \frac{V_{TH}\frac{\Delta I_S}{I_S}}{R_3+1/g_{m_{34}}}$$

$$V_{OS} = V_{TH}\frac{\Delta I_S}{I_S}\,\frac{1+g_m R_{12}}{1+g_m R_{34}} \rightsquigarrow \text{similar to noise}$$

If $\beta < +\infty$ then we have an additional offset term given by the mirror (not computed but easy to find)

11) CMRR and fully differential amplifiers



Differential mode $V_{IN}^+ - V_{IN}^- = V_{DIFF}$

Common mode $\frac{V_{IN}^+ + V_{IN}^-}{2} = V_{CM}$

For the output, there should be two gains, one diff. and one CM, that are orthogonal as well (not true)

$V_{IN,DIFF} \xrightarrow{A_{DD}} V_{OUT,DIFF}$

$V_{IN,CM} \xrightarrow{A_{CC}} V_{OUT,CM}$

→ We can build a matrix that connects input mode to output result

$\underline{A_{DD}} = g_m R \qquad \underline{A_{CC}} \simeq -\frac{R}{2r_o}$

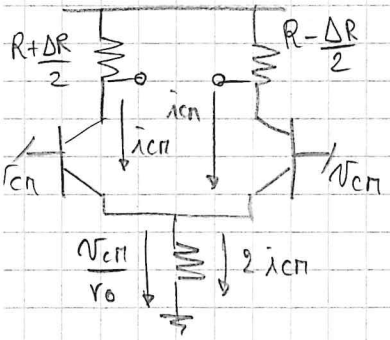
However, real circuits have non idealities → two unwanted gains:

$V_{IN,DIFF} \xrightarrow{A_{CD}} V_{OUT,DIFF}$

$V_{IN,CM} \xrightarrow{A_{DC}} V_{OUT,CM}$

→ Which is worst? A_{CD} because after the stage the CM disturbance will not be recognized as common mode anymore

A_{CD}

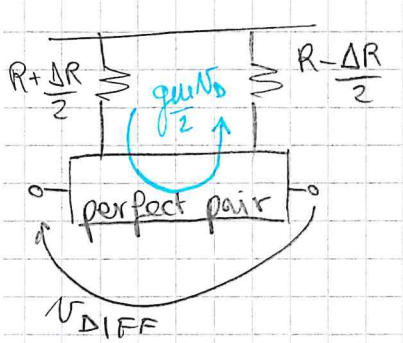


Consider a load mismatch and suppose that $2i_{CM}$ perfectly divides through Q_1, Q_2:

$\underline{A_{CD}} = -\frac{\Delta R}{2r_o}$ ↳ statistical result

Of course, we could have an emitter area mismatch

A_{DC}



$V_{OUT}^+ = \frac{g_m}{2} V_{DIFF} \left(R - \frac{\Delta R}{2}\right)$

$V_{OUT}^- = -\frac{g_m}{2} V_{DIFF} \left(R + \frac{\Delta R}{2}\right)$

$\underline{A_{DC}} = -\frac{g_m}{4} \Delta R$

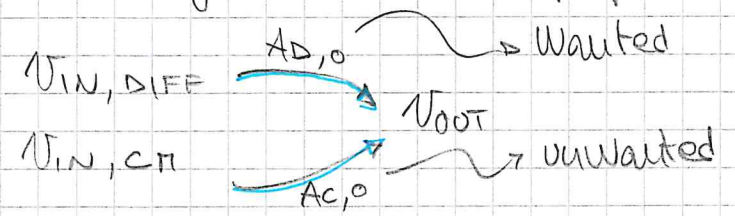
A_{DC} is generally less problematic because with fully diff amps we reject common mode contributions so the following stages will take care of this

Issues:

A_{CD} = following stages will recoguize this as a wanted differential signal

A_{DC} = can push the 2nd stage (and 1st stage as well) into bias conditions that decrease the performance

In single ended amplifiers the problem is even worse

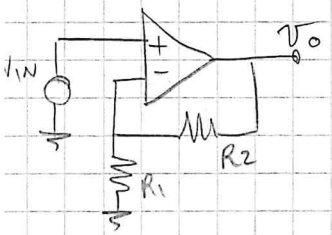


How do we limit $A_{C,D}$ and $A_{C,0}$? ① high impedance on tail gen ② perfect symmetry

② We never have it on single ended amps because of the current mirror!

Connection between openloop CMRR and closed loop circuits

$CMRR = \frac{A_{DD}}{A_{CC}}$ ↳ it's open loop but we always work with feedback circuits, why is it still useful?



↳ This configuration exerts a lot the CM signal Fully diff. amplifiers are better wrt. this.

Approximation: $V_\varepsilon \simeq 0$ for CM so $V_{CM} = \frac{V^+ + V^-}{2} = \frac{V_{IN} + V_{IN}}{2} = V_{IN}$

While $V_\varepsilon = V_{IN} - V_o \frac{R_1}{R_1 + R_2}$ for DM

$$V_{OUT} \simeq A_D V_\varepsilon + A_C V_{IN} \rightarrow \frac{V_{OUT}}{V_{IN}} \simeq \underbrace{\frac{A_D}{1 - G_{loop}}}_{①} + \underbrace{\frac{A_C}{1 - G_{loop}}}_{②}$$

Where $G_{loop} = -A_D \frac{R_1}{R_1 + R_2}$

① Wanted signal ② spurious signal

Figure of Merit: $CMRR = \frac{\text{Wanted}}{\text{spurious}} = \frac{A_D / (\cdots)}{A_C / (\cdots)} = \frac{A_D}{A_C}$ (① over the numerator, ② over the denominator)

And we end up with the open loop computed CMRR

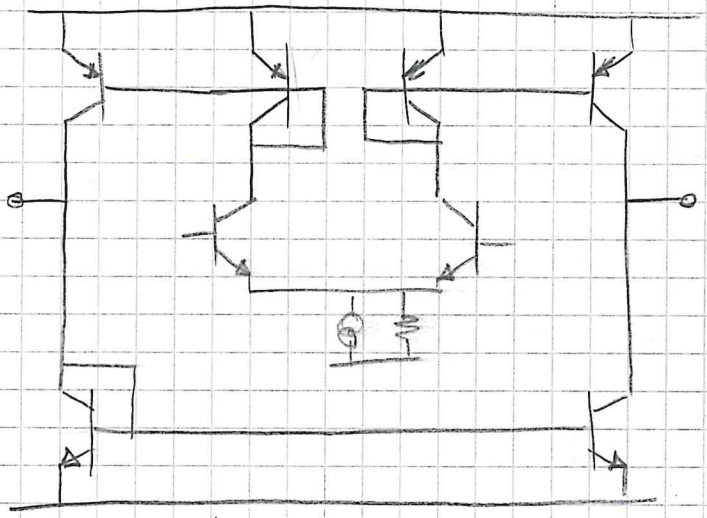
If we were wore rigorous:

$$V_\varepsilon = V_{IN} - V_{OUT}\frac{R_1}{R_1+R_2} \quad \text{and} \quad V_{CM,IN} = \frac{1}{2}\left[V_{IN} + V_{OUT}\frac{R_1}{R_1+R_2}\right]$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_D}{1+\left(\frac{R_1}{R_1+R_2}\right)\left(A_D - \frac{1}{2}A_C\right)} + \frac{1}{2}\,\frac{A_C}{1+\left(\frac{R_1}{R_1+R_2}\right)\left(A_D - \frac{1}{2}A_C\right)}$$

We're assuming that A_D, A_C are superimposable.
This is not true because A_{CM} can introduce distortion on the output with even harmonics!

Example of CMRR increase in bipolar tech



In this case the asymmetry is set by the npn mirror. Since npn transistors have higher β, this circuit has better CMRR because of the higher symmetry

Where's the tradeoff? More transistors = lower speed at the cost of better CMRR (lower systematic offset)

(2) Rule of thumb for computing CMRR

$CMRR \cong \frac{V_A}{V_{os}}$ → means we have a good tail generator
→ means we have low mismatches

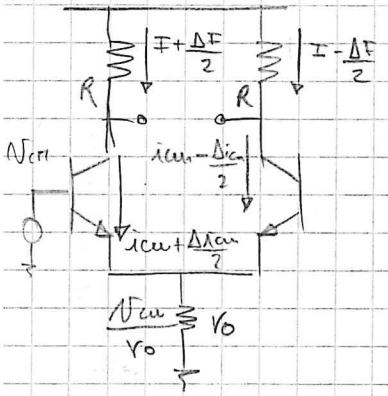
We can prove that CMRR is in this order of magnitude with some examples:

1° Consider the previously computed $A_{DD} = g_m R$ $A_{CC} = \frac{\Delta R}{2 r_o}$

then $CMRR = \frac{g_m R}{\frac{\Delta R}{2 r_o}} = \frac{I}{V_{TH}} \frac{2 r_o}{\frac{\Delta R}{R}} \cong \frac{V_A}{V_{os}}$

This is the most obvious case but other circuits will show a CMRR that is in the same order of magnitude.

2° Consider a mismatch on I_s of the diff. pair:



$$\frac{\Delta i_{cm}}{i_{cm}} = \frac{g_{m1} - g_{m2}}{g_{m1} + g_{m2}} \sim \frac{g_{m1} - g_{m2}}{2 g_{m1}} \sim \frac{\left(I + \frac{\Delta I}{2}\right) - \left(I - \frac{\Delta I}{2}\right)}{2I}$$

$$\cong \frac{\Delta I}{2I} = \frac{\Delta I_S}{2 I_S}$$

$$CMRR = \frac{g_m R}{\frac{1}{r_o}\left(\frac{\Delta I_S}{2 I_S}\right) R} \cong \frac{V_A}{V_{os}}$$

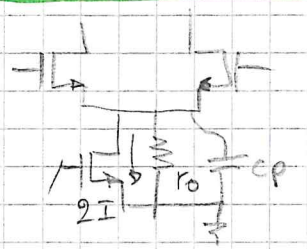
3° Consider a β mismatch on the mirror, then

$$CMRR = \frac{g_m}{\frac{1}{2 r_o} \cdot \frac{2}{\beta}} = \frac{2 r_o I}{V_{TH} 2/\beta} \cong V_A / V_{os}$$

↳ see previous computations

(Note: in example 2 see analog circuit design notes on question 17 on CMRR statist/determin. for a rigurous computation)

13) CMRR variation with frequency



At HF we experience the effect of C_{par} which has a fairly large value.

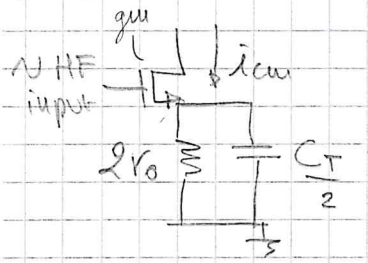
In order to generate $2I$ current, the tail gen must have:

① Large $\left(\frac{W}{L}\right)$ ② low V_{ov} (because of voltage dynamic/headroom)

③ large r_o for good CMRR → Large V_A → $L_{tail\ gen} \gg L_{min\ process}$

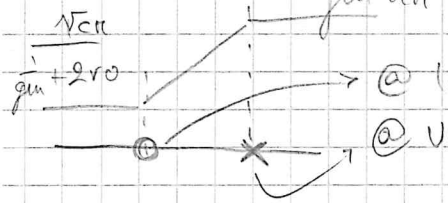
→ Since we meet ①, ③ requirements → WL = Area is large and so does the $C_{parasitic\ tail}$

Consider the CM half circuit:



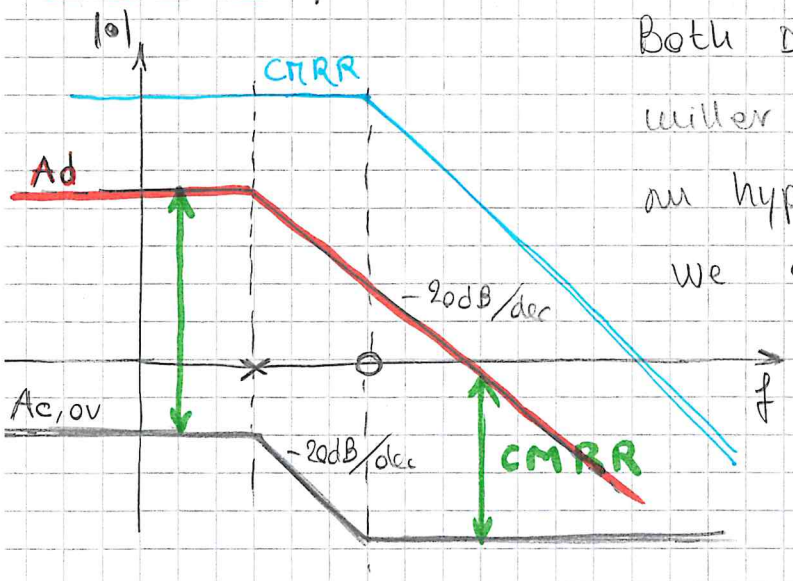
$$i_{cm} = \frac{V_{CM}}{\frac{1}{g_m} + 2r_o} \cdot \frac{1 + s\frac{C_T}{2} \cdot 2r_o}{1 + s\frac{C_T}{2}\left(2r_o \,//\, 1/g_m\right)}$$

$$= \frac{V_{CM}}{\frac{1}{g_m} + 2r_o} \cdot \frac{1 + sC_T r_o}{1 + s\frac{C_T}{2} \cdot 1/g_m}$$

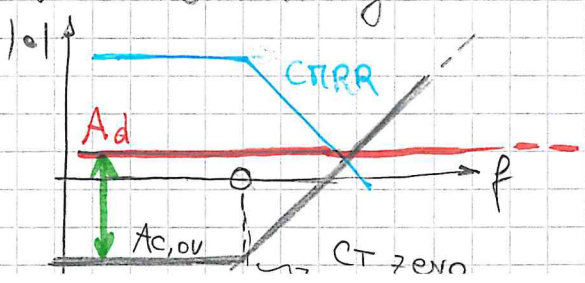


→ We don't care about the HF pole, we see that i_{CM} ↗ pretty soon because C_T is large in value

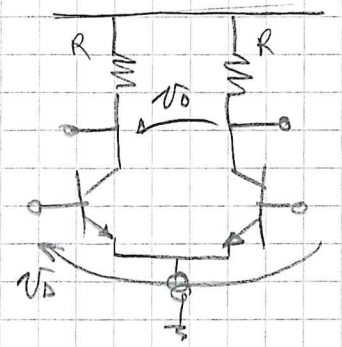
DM + CM plot:

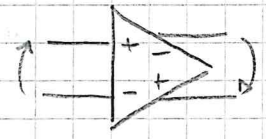


Both DM and CM gain see the miller pole (this plot is V_{OUT} of an hypothetical 2nd stage). If we considered just the $i_{cc\,OUT}$ of the 1st stage, we would see the same result but with something like this:



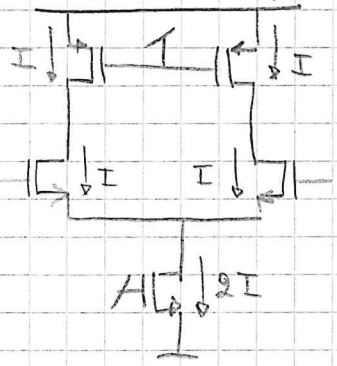
14) Fully differential amplifier





↳ We do not care much about the gain sign, we can easily swap directions (helpful for filter implementation)

Most fully diff. implementations are CMOS. Consider active loads

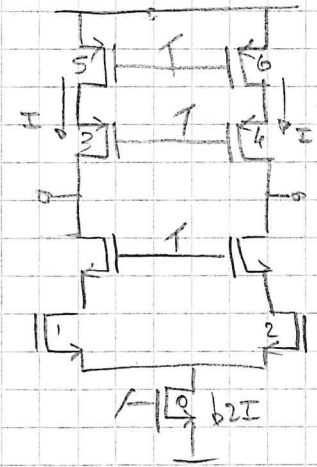


Issue: match currents of the two back to back generators by design → We need to dissipate more power to add a Common Mode Feedback (CMF) circuit.

What's the point of fully diff. then?

- PSRR is better because of more symmetry
- CM disturbances are rejected (Note: CM disturbs can either be externals or directly related to the circuit topology. e.g.: SW cap. circuits exert the CM a lot) → CMRR ↗
- Positive/Negative gain for free (single ended would need an additional inverting stage)

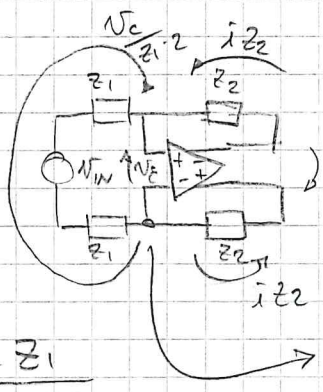
Fully diff telescopic amp



$I_5 = I_6 = I$ need to be matched to $I_0 = 2I$

gain $A_{DD} = \frac{g_m}{2} V_b \left[2 r_{op} g_m r_{op}\right] // \left[2 r_{on} g_m r_{on}\right]$

Note: Rout changes for DM and CM

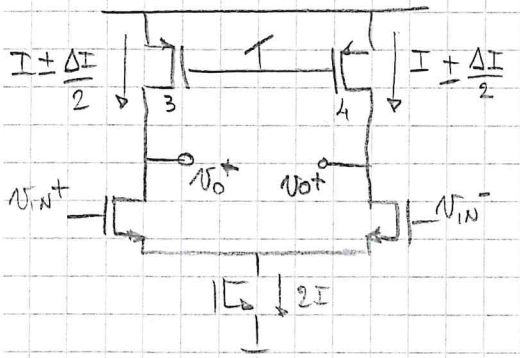


$$\Rightarrow \frac{V_o}{V_s} = \frac{1}{2Z_1} \cdot 2Z_2 = \frac{Z_2}{Z_1}$$

$$G_{loop} = -A_{DD} \cdot \frac{2Z_1}{2Z_1 + 2Z_2}$$

Note: $V_{CM,in}$ will be set by both output CMF and input generator CM voltage!

15) DM and CM biasing errors in fully diff amplifiers



1) Differential error (DME)

$I_{M3} = I + \frac{\Delta I}{2}$ $\quad I_{M4} = I - \frac{\Delta I}{2}$

We will experience output saturation

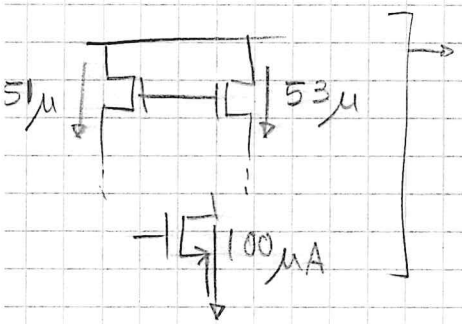
V_{out}^- $\quad V_{out}^+$ → A_{DD} issue (we will correct it with feedback)

We can say that DME is a contribution to the offset

2) Common mode error (CME):

$I_{M3} = I + \frac{\Delta I}{2}$ $\quad I_{M4} = I + \frac{\Delta I}{2}$ → since it's a common mode contribution, it's a A_{CC} issue and therefore feedback can't correct it → CMF!

We divide DME and CME as follows:

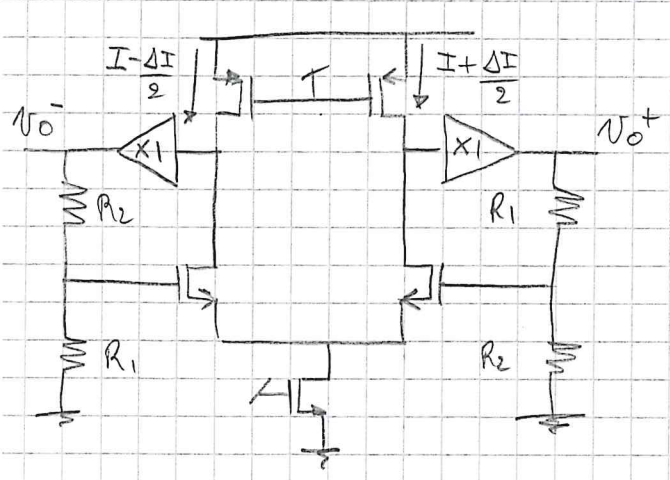


↓ 50μA ↓ 50μA → ideal I_{M5}, I_{M6}

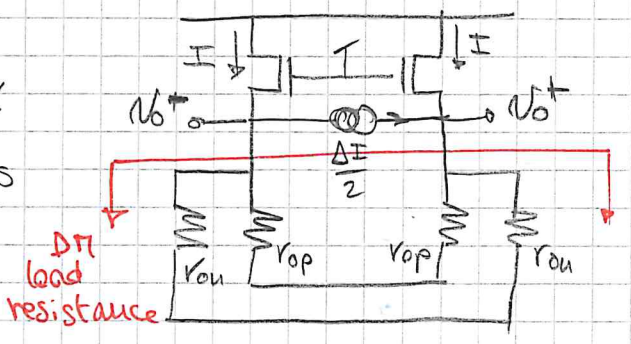
↓ 2μA ↓ 2μA → CME

↑ μA ↓ μA → DME

Differential error correction through feedback



We can equivalently model the DTE as

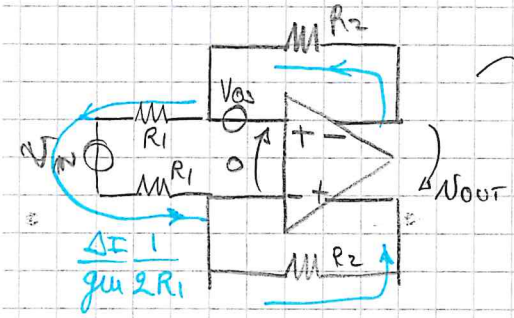


$$V_{OUT\,DIFF}\Big|_{OL} = \frac{\Delta I}{2}\left[2r_{op} /\!/ 2r_{on}\right]$$

$$|G_{loop}(0)| = \frac{g_m}{2}\left[2r_{op} /\!/ 2r_{on}\right]\frac{R_1}{R_1+R_2}$$

$$V_{OUT\,DIFF}\Big|_{CL} = \frac{\Delta I\,[r_{op} /\!/ r_{on}]}{1+g_m[r_{op} /\!/ r_{ON}]\frac{R_1}{R_1+R_2}} = \underbrace{\frac{\Delta I}{g_m}\left(1+\frac{R_2}{R_1}\right)}_{\text{Ideal gain}}\underbrace{\frac{1}{1+\frac{1}{G_{loop}}}}_{\text{correction}}$$

Note: $\frac{\Delta I}{g_m}$ = input "equivalent offset" generator needed to unbalance the stage and correct the DTE



$$V_{OUT}\Big|_{V_{OS}} = V_{OS} + \frac{V_{OS}}{2R_1}\cdot 2R_2 = V_{OS}\left(1+\frac{R_2}{R_1}\right) = \frac{\Delta I}{g_m}\left(1+\frac{R_2}{R_1}\right)$$

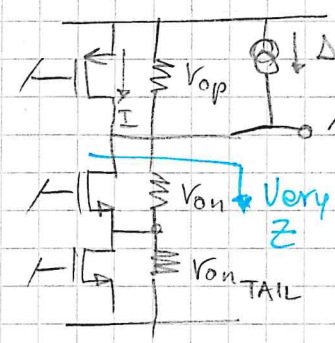
$$V_{OUT}\Big|_{V_{IN}} = V_{IN}\,\frac{R_2}{R_1}$$

Diff gain differs from offset gain

Common mode error (correction: Let's see)

Consider the same feedback circuit of DME but now:

We now consider Acc for computing this ΔI contribution. $\rightarrow V_o^+$ and $\rightarrow V_o^-$

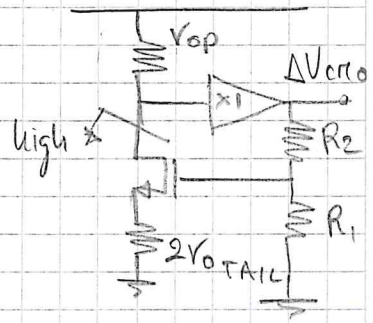


Very high Z

Consider the half CM circuit, Vout is:

$$V_o = \Delta I \left[r_{op} \,/\!/\, r_{on}(g_m r_{o_{TAIL}}) \right] \cong \Delta I\, r_{op}$$

We now consider the R_1, R_2 feedback:



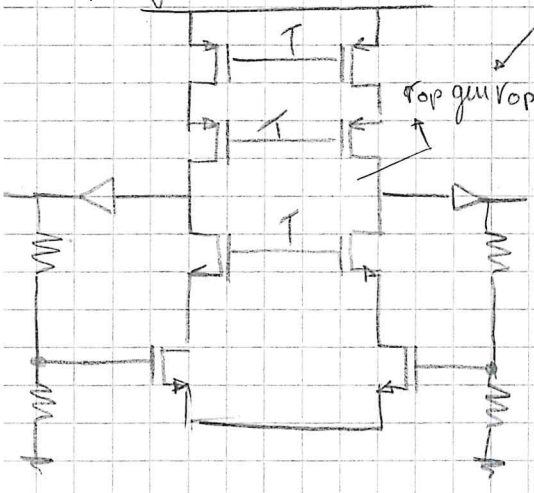
So

$$\Delta V_{cm_{OUT}} \cong \Delta I r_{op} - \Delta V_{cm_{OUT}} \left(\frac{R_1}{R_1+R_2} \right) \frac{r_{op}}{2r_{O_{TAIL}}}$$

$$= \Delta I \; \frac{r_{op}}{1+\left(\frac{R_1}{R_1+R_2}\right)\frac{r_{op}}{2r_{OT}}} \quad \text{Acc}$$

$$G_{loop}|_{CM} = -\left(\frac{R_1}{R_1+R_2}\right)\cdot\frac{r_{op}}{2r_{OT}} \rightarrow r_{op} \sim r_{OT} \Rightarrow$$ This "common mode Gloop" is very poor → output still saturates

We may try to increase the loop gain with a telescopic configuration:



$$\text{Acc} = -\frac{1}{2r_{OT}}\left(r_{op} g_m r_{op}\right)$$

Now Acc is μ (~100) times larger than the normal amplifier. Is it enough? NO:

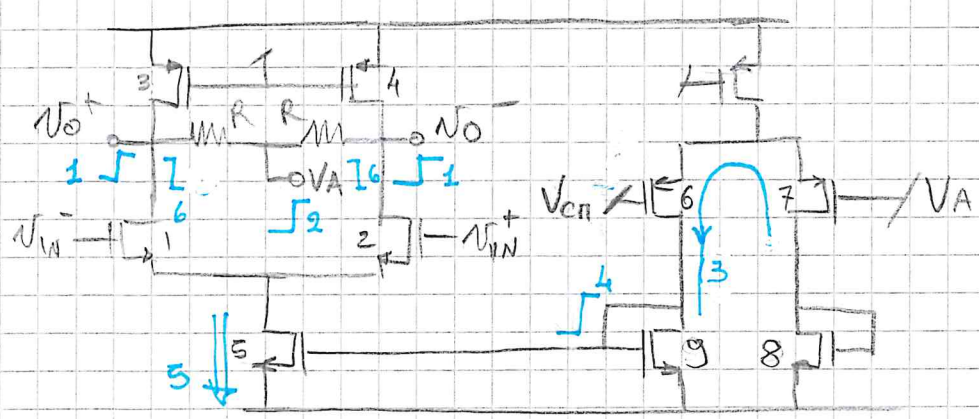
$$\Delta V_{cm_{OUT}} = \Delta I \; \frac{\overset{①}{g_m r_{op}^2}}{1+\frac{R_1}{R_1+R_2}\overset{②}{\frac{g_m r_{op}^2}{r_{OT}}}}$$

Nothing changes because ① and ② increase by the same magnitude:

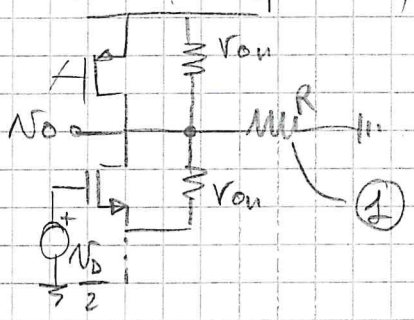
$$\Delta V_{OUT} \cong \Delta I\, r_{OT}\left(\frac{R_2}{R_1}+1\right)$$ → r_{OT} is large → feedback is not enough

We need to devise a feedback that acts on the CM only. The solution for CME is thus the CMF.

16) Common Mode Feedback (CMF)



DM circuit (partial)



$$A_{DD} = \frac{g_{M12}}{2}\left(2R \,//\, 2r_{op34} \,//\, 2r_{on12}\right)$$

↳ (1) there's R contribution

We can set $R \gg r_o$ because no bias current flows through it

1) V_o^+ V_o^- rise because of ΔI

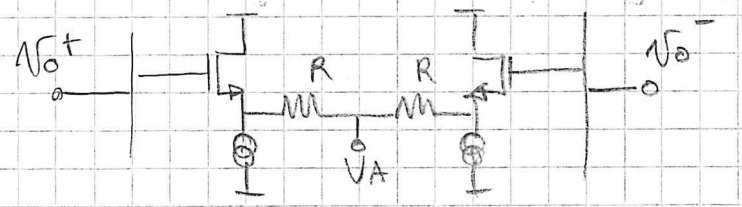
2) V_A rises as well

3) A current is generated on the CMF branch and

5) Tail generator increases its current because of (4)

6) Negative voltage step compensates (1) to have the correct $V_A = V_{CM}$ as it is set by the CMF circuit

Real implementations sometimes use voltage buffers to get high A_{DD}:



We buffer R from $r_{op} // r_{on}$ but we get

- more power dissipation
- less linearity than just R because of the active buffers (troublesome because V_o swing is large and a nonlinear CMF with large swings will move the $V_{CM\,OUT}$ because of a differential signal only → A_{DC} nonlinear contribution that depends on V_{OUT} amplitude!)

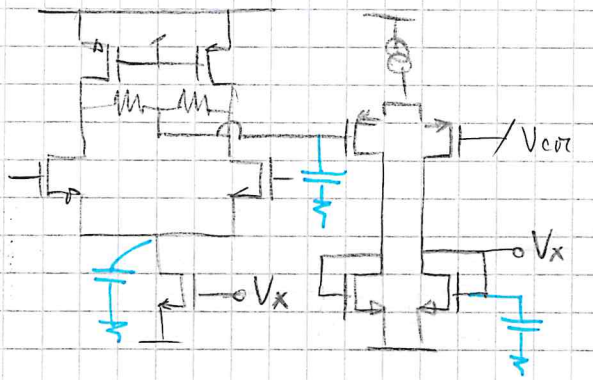
$G_{loop_{CMF}}(0) = -\frac{gm_{67}}{2} \cdot \frac{1}{gm_5} \cdot gm_5 \cdot r_{o3,4}$ ~ in the order of a μ

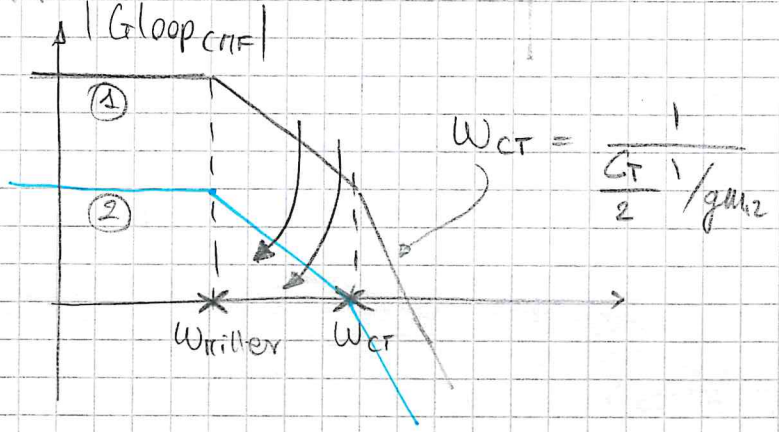
Is this loop asymptotically stable? Both CM, DM see different impedances:

$$\omega_{miller}\Big|_{DM} = \frac{1}{\frac{C_0}{2}(2R \,//\, 2r_{op} \,//\, 2r_{on})} = \frac{1}{C_0(R \,//\, r_{op} \,//\, r_{on})} \approx \frac{2}{C_0 r_{op}}$$

$$\omega_{miller}\Big|_{CM} = \frac{1}{C_0 r_{op}}$$

DM, CM poles differ by a factor 2, 3 typically, but CM has 3 extra poles at least!

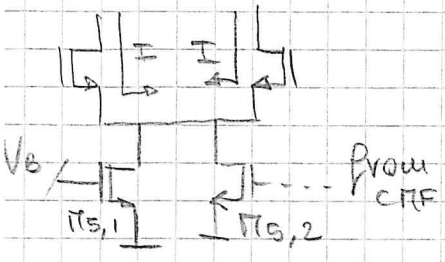


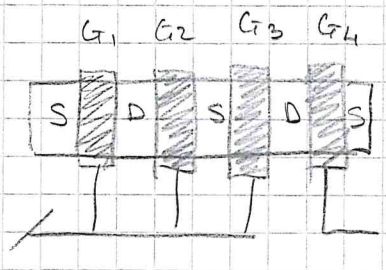


① $G_{loop_{CM}}$ typically shows two poles in BW → it can generate oscillations of the CM.

② To have just one pole in BW, we cannot do much other than lowering $G_{loop_{CM}}$ (it's the only correction that does not affect A_{DD} which is more critical)

How do we implement this lower gain? Double tail:





Remember that lower $G_{loop_{CMF}}(0)$ → lower accuracy

For example $\left(\frac{W}{L}\right)_{M_{5,2}} = \frac{1}{4}\left(\frac{W}{L}\right)_{M_5}$

Compute now the output swing due to a ΔI under the effect of the CMF

$$\Delta V_{CM\,OUT} = \frac{\Delta I \, r_{op}}{1 + g_{m6,7} \cdot \frac{1}{g_{m3}} \cdot \frac{g_{m5}}{4} \cdot r_{op}}$$

$\rightarrow g_{m5,2} = \frac{1}{4} g_{m5}$

$$G_{loop}(0)\big|_{CMF} = -g_{m6,7} \cdot \frac{1}{g_{m3}} \cdot \frac{g_{m5}}{4} r_{op} \sim g_m r_o \rightarrow 1 \text{ order of magnitude}$$

We can clude that:

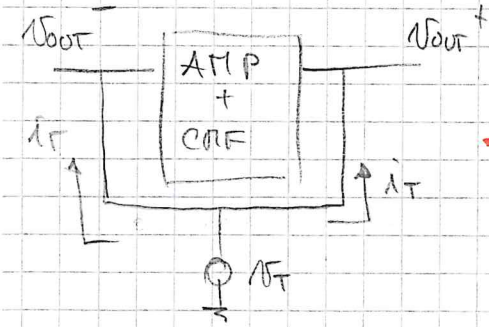
$$\frac{\Delta V_{CM\,OUT}}{\Delta I} \simeq \frac{1}{\frac{g_{m6}}{4} \cdot \frac{g_{m5}}{g_{m3}}}$$

Compute now $\Delta V_{CM\,OUT}$ given an input CM signal:

$$\frac{\Delta V_{CM\,OUT}}{\Delta V_{CM\,IN}} = \frac{\frac{r_{op}}{2 r_{OT}}}{1 + G_{loop}(0)\big|_{CMF}} \simeq \frac{1}{2 r_{OT} \frac{g_{m6,7}}{4} \frac{g_{m5}}{g_{m3}}}$$

CM transfer is negligible, CMF is devised for setting the bias point. Of course Acc will be slightly better as well.

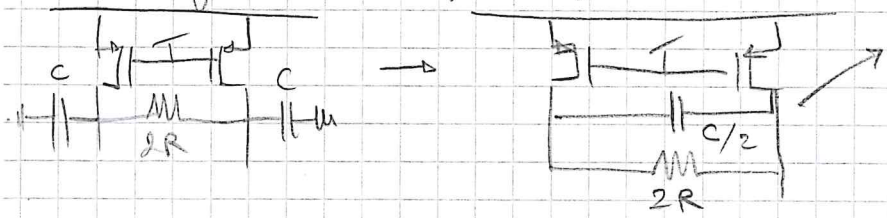
We can view this from a $Z_{OUT}\big|_{CM}$ change:



$$Z_{OUT}\big|_{CM} = \frac{V_T}{i_T} \begin{cases} \simeq r_{op} \text{ if OL } ① \\ \simeq \frac{r_{op}}{1 + g_m \cdot r_{op}} \text{ in CL } ② \end{cases}$$

By putting the numbers in ①, ② they could differ by one order of magnitude.

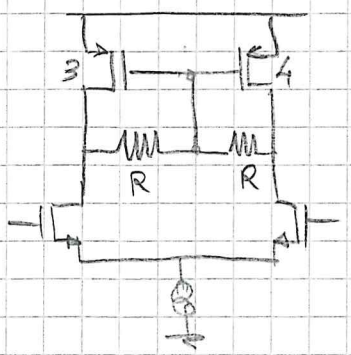
Removing miller pole from CM transfer



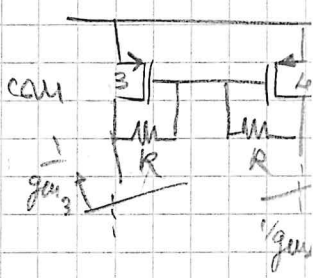
capacitor is seen by A_{DD} not seen in Acc

We usually don't remove the pole at all because we want a stable CMF loop

Alternative CMF current control node



With a classic fully diff amp, we can directly connect V_A to $V_{G3,4}$.



In CM (think about it in terms of CM half circuit) we will get a $1/g_m$ impedance instead of r_{op}

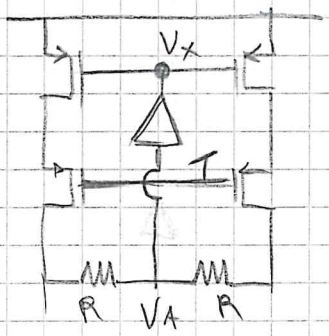
$$\frac{V_{OUT}}{V_{CM}} = -\frac{1}{2r_{OT}} \cdot \frac{1}{g_{m3,4}}$$ → transdiode!

$$W_{miller}\Big|_{DM} = \frac{1}{\frac{C_\Pi}{2}\left(2R \,//\, 2r_{on} \,//\, 2r_{on}\right)}$$ ↳ Unchanged

$$W_{miller}\Big|_{CM} = \frac{1}{C_\Pi \cdot 1/g_{m3,4}}$$

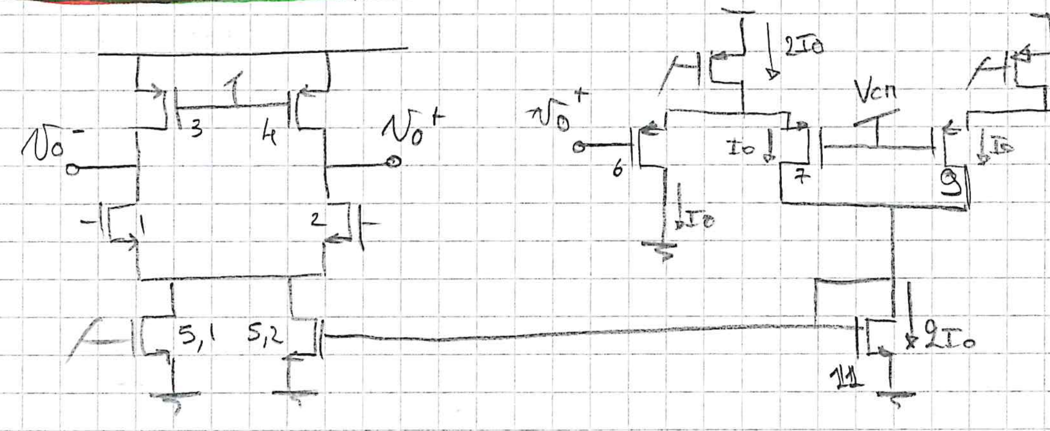
Therefore $A_{c,c}$ and $W_{miller}|_{CM}$ changed!

For telescopic cascodes we'd need a level shifter:



Connecting V_A to V_X directly would break the cascoded transistors voltage headroom.

17) Example of an active CMF circuit



Instead of a resistive sensing, we use a double mosfet pair (output load is now an added gate capacitance of the CMF)

Working principle is trivial.

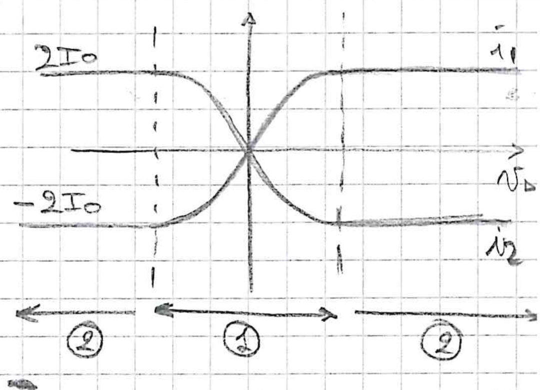
$$G_{loop}(0)\Big|_{CMF} = -\frac{g_{m6,8}}{2}\cdot 2\cdot\frac{1}{g_{m11}}\cdot g_{m5,2}\cdot\frac{1}{2}\, R_{OUT}\Big|_{CM}$$

($R_{OUT}|_{CM}$ → $r_{op3,4}$; $\frac{1}{2}$ → current division)

$V_{CM\,OUT} = V_{CM} + \Delta V_{CM\,OUT}$ (V_{CM} set by design)

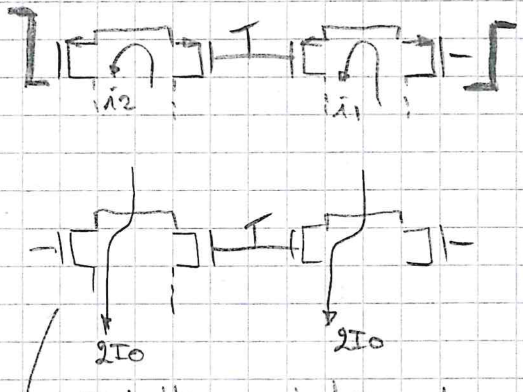
$$\Delta V_{CM\,OUT} = \frac{\Delta I\ \cancel{R_{OUT\,CM}}}{1+\frac{g_m}{g_m}g_m\cdot\frac{1}{2}\cancel{R_{OUT\,CM}}} \simeq \frac{\Delta I}{\frac{g_{m6,8}}{g_{m11}}\cdot\frac{1}{2}g_{m5}}$$

→ few mV typ value



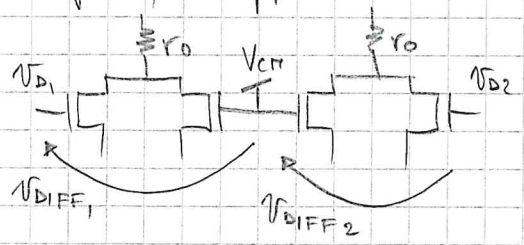
Even with large output voltage swing:

1. large v_D signal still has symmetrical i_1 and i_2
2. When $v_D > \sim V_{OV}$ we need to be careful because the stage is totally unbalanced and the CMF cannot react to CM swings anymore. Moreover, with large v_D swings, g_m change and $G_{loop}|_{CM}$ decreases



→ Totally unbalanced stage

Notice that since one end of the pair is fixed to V_{CM}, a fully differential V_o^+, V_o^- will still exert both DM and CM:

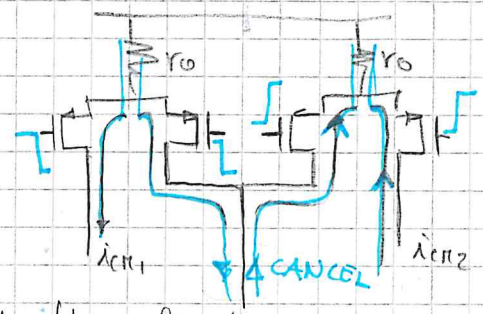


$$V_{DIFF1} = V_{D1} - V_{CM}$$

$$V_{CM1} = \frac{V_{D1} + V_{CM}}{2}$$

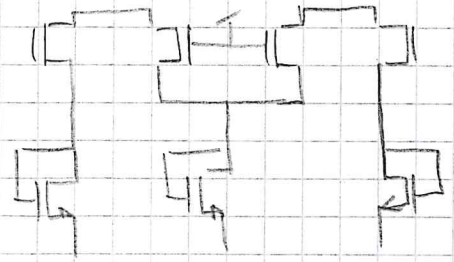
→ same for V_{DIFF2}, V_{CM2}

See the CM current contribution:
at first order, since V_{CM1} and V_{CM2} are in opposite directions, i_{CM1} and i_{CM2} are canceled through M_{11} branch (to first order)

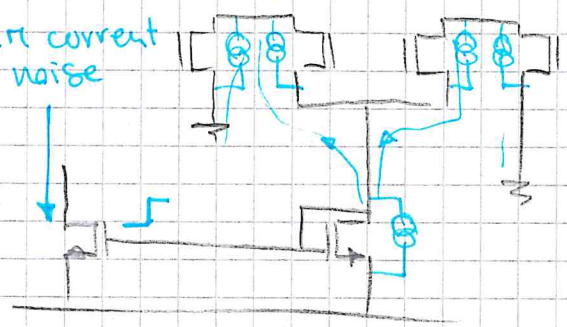


Other notes:

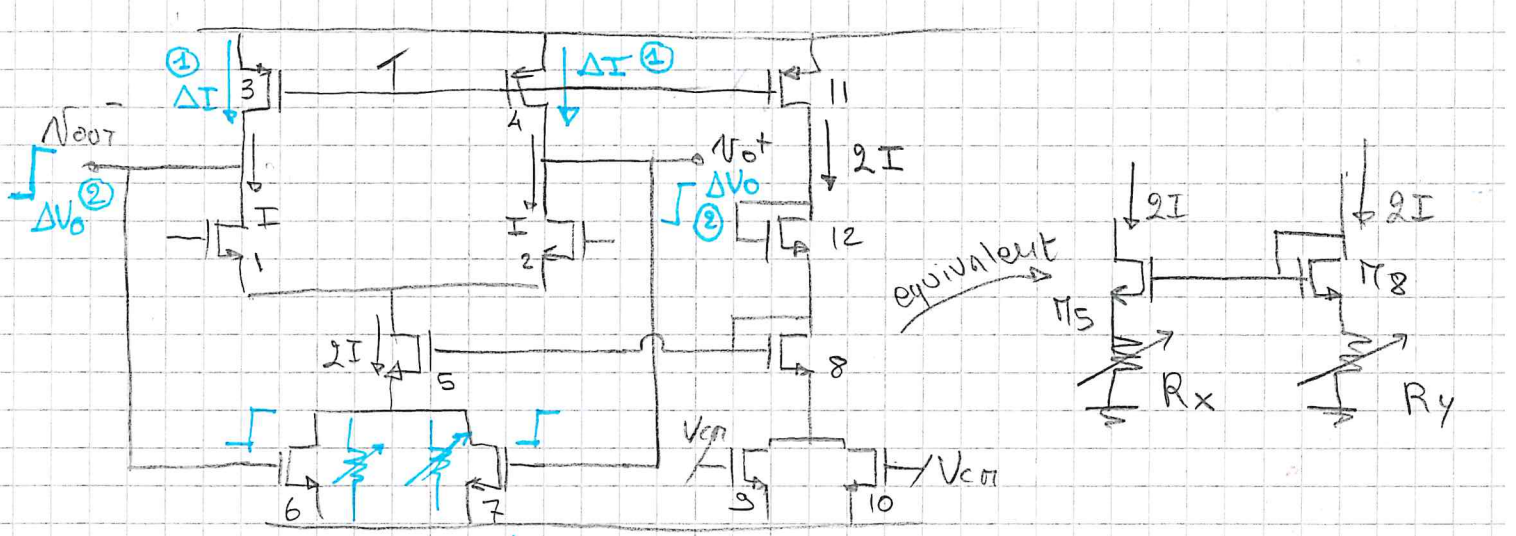
- Sources of the double pairs have 2nd harmonics that are in phase → contribution to M_{11} current
- Originally designed not to have resistive loads on A_{DD}
- Real implementations have dummy loads to balance the V_{DS} for better symmetry:



- Any noise coming from the CMF double pair and propagating back to the amplifier through M_{11} gives a common mode contribution because it drives a tail generator gate:



18) Example of a low power CMF



↳ r_{ON} changes (ohmic) (decreases if ΔV_o is positive)

M_6, M_7 are for sure in ohmic region because $V_G \gg V_T$

Circuit adjusts the bias current through the use of voltage controlled resistors in the "equivalent" degenerated mirror. The resistors $R_x = R_{ON}|_{M_6} // R_{ON}|_{M_7}$ $R_y = R_{ON}|_{M_9} // R_{ON}|_{M}$

Issue: large V_{OUT} swing will turn off M_6, M_7 → We can't have large output voltage:

$$I = \mu_n C_{ox}' \left(\frac{W}{L}\right)_{6,7} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

↳ linear region

$$G = \frac{I}{V_{DS}} \approx \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_T)$$

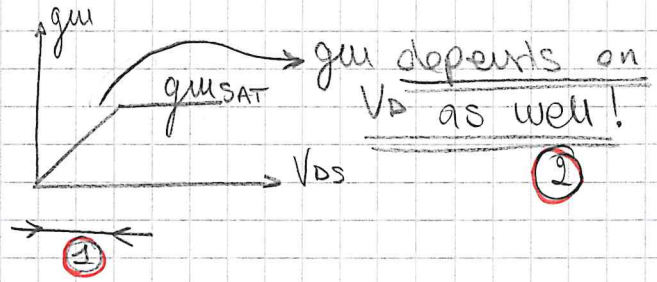
↳ conductance

$$R_x = \frac{1}{\mu C_{ox} \left(\frac{W}{L}\right)_6 (V_{GS} - V_T)_6 + \mu_n C_{ox} \left(\frac{W}{L}\right)_7 (V_{GS} - V_T)_7}$$

$(V_{GS} - V_T)_6$: $+\Delta V$ ↑ $(V_{GS} - V_T)_7$: $-\Delta V$ ↓

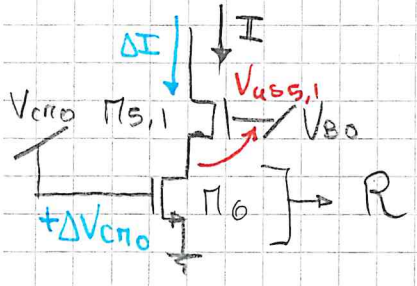
Compute the $G_{loop}(0)|_{CMF}$:

$$g_{m\,6,7}\Big|_{ohmic} = \frac{\partial I}{\partial V_{GS}} = \mu_n C_{ox} \left(\frac{W}{L}\right)_{6,7} V_{DS}$$



We can easily estimate that $\frac{\Delta V_{CM}}{\Delta I} \approx 1/g_{m\,6,7}$ → the larger the g_m, the better. However our working region is (1), thus g_m is small. Moreover, $G_{loop}(0)|_{CMF}$ changes with V_{DS} → (2)

For the sake of completeness, let's be rigurous on Gloop (0) cr



If I move the M_6 gate by ΔV_{cm0}, how much is ΔI?

bias M_5 voltage

$$I R + V_{GS_{5,1}} = V_{BO}$$

I ← bias current

$\frac{1}{g_{m5,1}}$

$$I R + V_T + \sqrt{\frac{I}{\kappa' \left(\frac{W}{L}\right)_{5,1}}} = V_{BO} \xrightarrow[\Delta I]{\text{small}} (dI)R + I(dR) \frac{1}{2\sqrt{\kappa \left(\frac{W}{L}\right)_{5,1}}} (dI) = 0$$

(1)

$$dI = \frac{-dR}{\frac{1}{g_{m5,1}} + R} I \rightarrow \text{expected degenerated mirror result}$$

$\frac{1}{g_{m5,1}}$ → Approx to be in linear region

$$R \simeq \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_6 V_{ov_6}} \quad \text{where } V_{ov_6} = (V_{GS} - V_T)_6 = (V_{cm0} - V_T)_6$$

If we have $\Delta V_{cm0} \rightarrow \Delta V_{GS}|_{M_6}$, so for a small change dV_{cm0}:

$$dR \simeq -R \frac{dV_{cm0}}{(V_{GS} - V_T)_6} \longrightarrow \text{Now plug this into (1)}$$

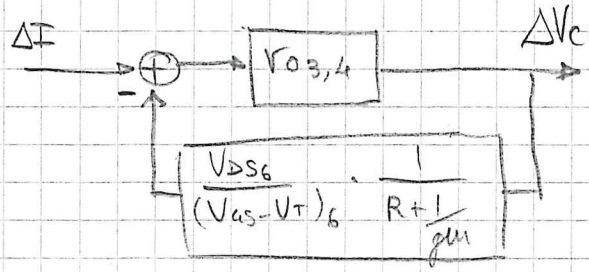
$I \cdot R$

$$dI = \frac{IR}{R + 1/g_{m5,1}} \cdot \frac{dV_{cm0}}{(V_{GS} - V_T)_6} = \frac{V_{DS_6}}{(V_{GS} - V_T)_6} \cdot \frac{dV_{cm0}}{R + 1/g_{m5,1}}$$

Remarks:

- If $V_{cm0} \nearrow \Rightarrow I \nearrow$ - bias current I is insensitive to small V_{DS} change

The final $G_{loop}(0)|_{CMF}$ is:



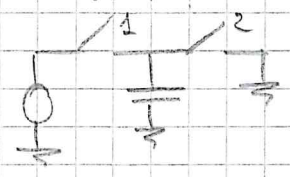
$$\frac{\Delta V_{cm0}}{\Delta I} \approx \left(R + \frac{1}{g_{m5,1}}\right) \frac{(V_{GS} - V_T)_6}{V_{DS_6}}$$

If we neglect $1/g_{m5,1}$, then:

$$\frac{\Delta V_{cm0}}{\Delta I} \approx \frac{1}{\mu C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_T)_6} \cdot \frac{(V_{GS} - V_T)_6}{V_{DS_6}} = \frac{1}{g_{m6,7}} \longrightarrow \text{We finally (brutal approx.)}$$

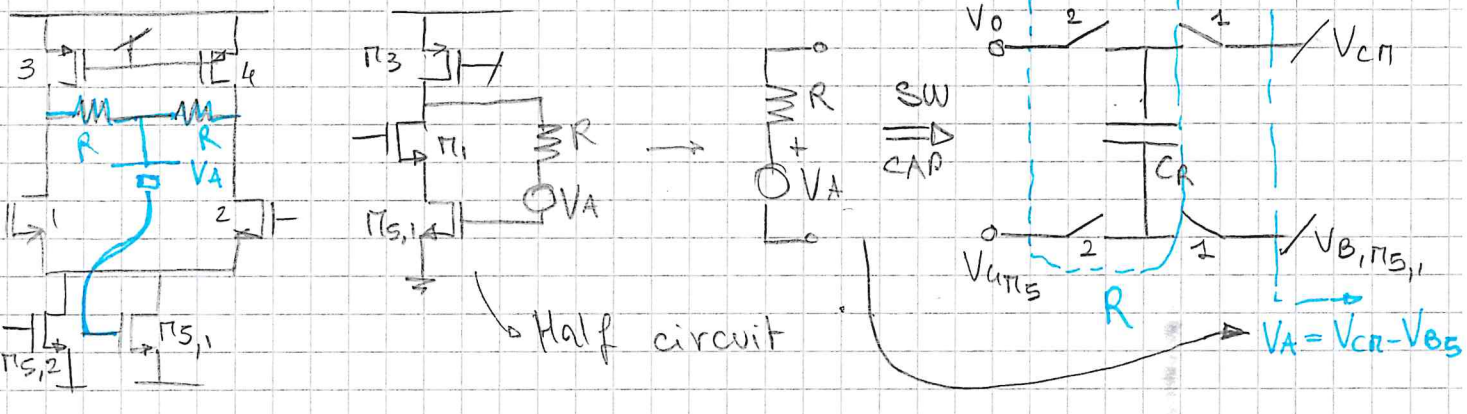
demonstrated the previously mentioned estimation

Since in sw. cap filters we already need sw and clock design, we can think of a sw. cap CMF circuit too!

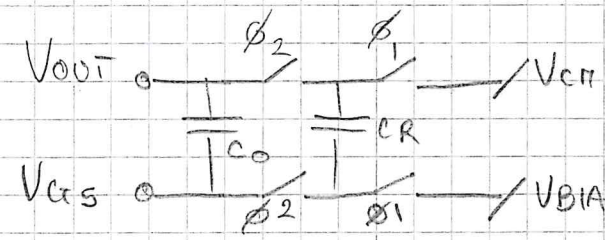


$$\frac{Q}{T_S} = \frac{cV_0}{T_S} = \bar{I} \rightarrow \frac{T_S}{c} = \text{Requivalent}$$

Note: sw cap CMF is useless in circuits w/o sw cap. because we wouldn't need clock and sw design. Look at the circuit:

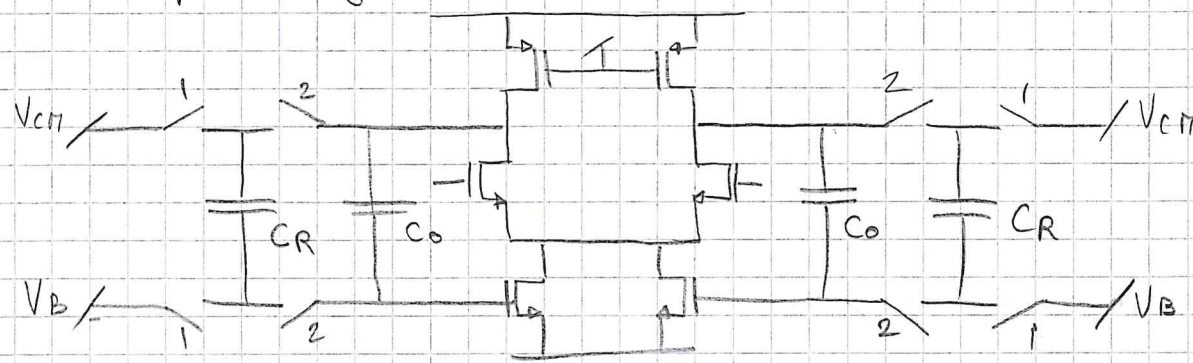


To properly drive $\Pi_{5,1}$ gate with the resistor sensing, we need a voltage (constant gen.) shifter V_A. When looking at the half circuit we see that we need an equivalent resistor and battery which can be easily implemented using sw capacitors. However, during phase 1 (ϕ_1), V_{GS} and V_{OUT} are floating → connect another capacitor



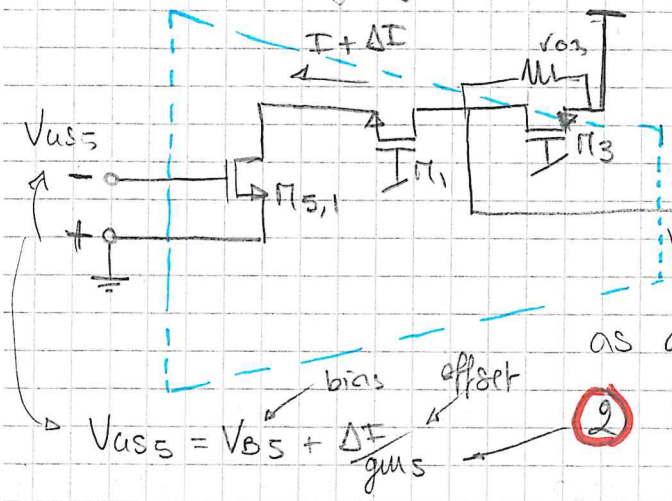
Note: it's an equivalent resistor. Even though we use capacitors we still dissipate power on average

And the following is the complete structure:



To properly compute istantaneous and average power dissipation and $G_{loop}|_{CMF}$ stability, we always use simulations.

How it works. It's better to analyze a ΔI response using (and rearranging) the half circuit and seeing it as an OTA:



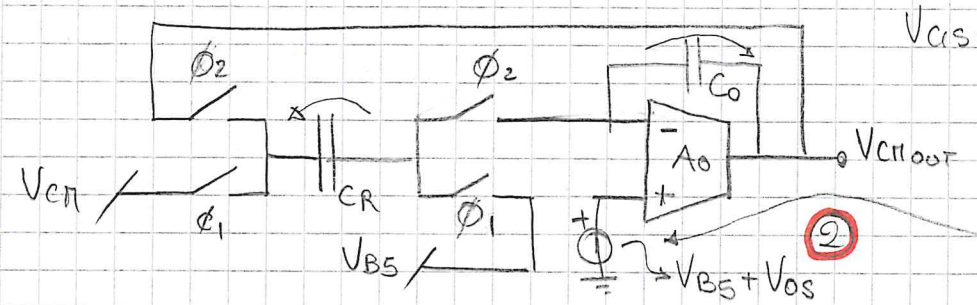
$A_0 = -g_{m5,1} \cdot r_{o3}$, $v_{IN}^+ - v_{IN}^- = V_{GS5}$

V_{GS5} takes into account the bias current I and the added mismatch ΔI, which can be seen at the gate as an offset on top of V_{B5}:

$$V_{GS5} = V_{B5} + \frac{\Delta I}{g_{m5}}$$ (bias, offset) (2)

$$\Delta V_{GS} = \frac{\Delta I}{g_{m5,1}} = \text{seen as offset}$$ (1)

To simplify the discussion, assume $A_0 \to +\infty$:



V_{GS5} is modeled as a generator on v_{IN}^+ of the OTA:

Assume that all charge is transferred $Q_{TOT\,\phi_1} = Q_{TOT\,\phi_2}$

$$Q_{TOT\,\phi_1} \to (V_{CM} - V_B) C_R + (V_{CM_{OUT}} - V_B - V_{OS}) C_0$$

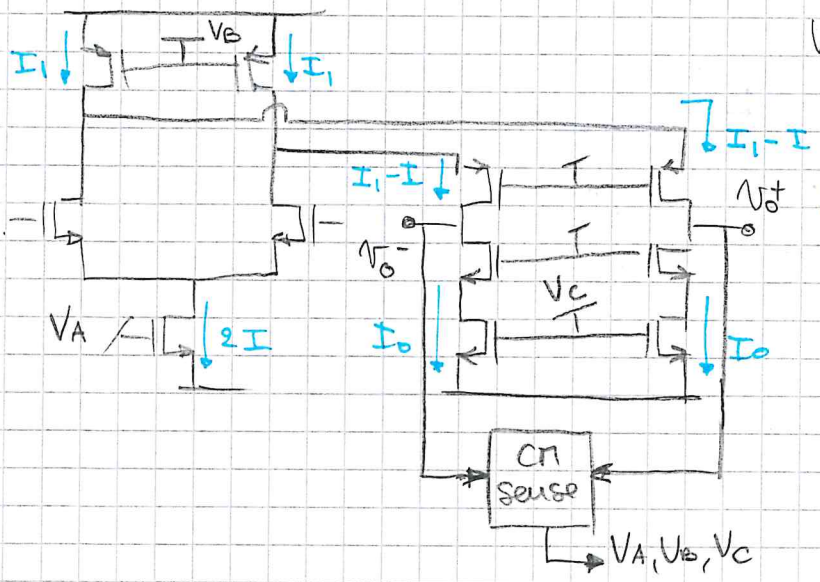
$$Q_{TOT\,\phi_2} \to (C_R + C_0)(V_{CM_{OUT}} - V_B - V_{OS})$$

$V_{CM_{OUT}} = V_{CM} + V_{OS}$

Since we can select whatever shift V_A, this sw.cap CMF is suitable for telescopic and folded cascode amplifiers

Note: the "usual result" (1) comes from the equivalent analysis of the linear circuit with just R and V_A battery. This last sw.cap analysis shows that this ΔI compensation can be adjusted with sw.caps instead

20) Fully differential folded cascode amplifier



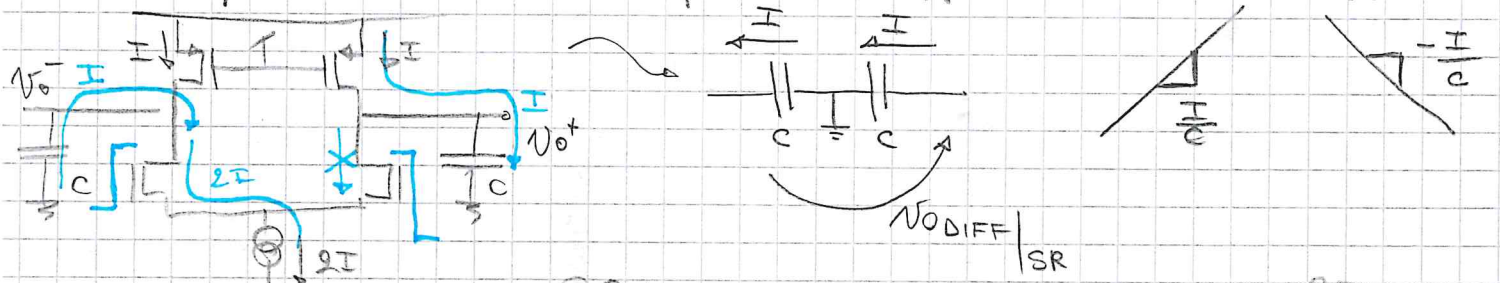
We can control the bias current in V_A, V_B, V_C.

$I_1 > I$ and $I_o = I_1 - I$

See analog circuit design notes for analysis

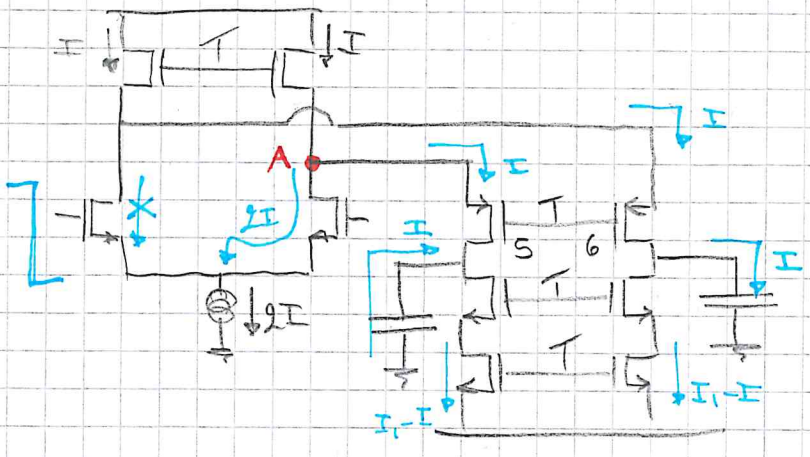
Slew Rate analysis

Recall for a standard fully diff amp:



$$SR|_{single} = \frac{I}{C} \qquad SR|_{fully\ diff} = \frac{2I}{C}$$

For a folded cascode:

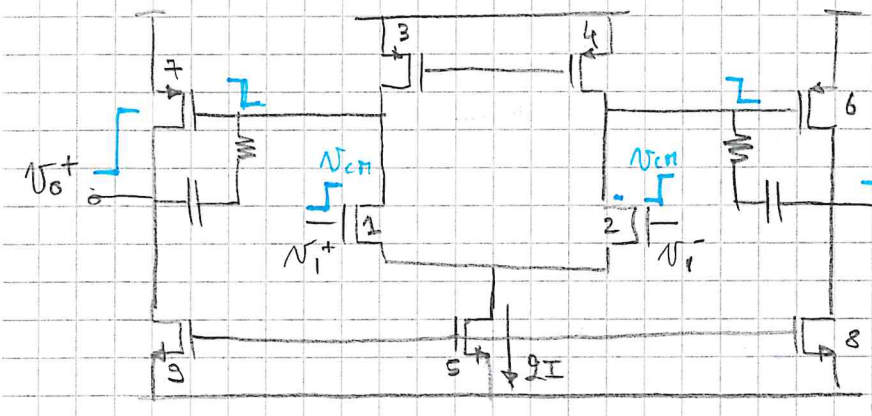


Note: $I_1 > 2I$ because $I_1 - 2I > 0$ on node A, otherwise $M_{5,6}$ would "shut off"

$$SR_{DIFF} = \frac{2I}{C}$$

In reality, even with $I_1 - 2I < 0$ SR works but with lower slope. Moreover, since the M_5, M_6 have to reverse the charge conditions (i.e: switch drain with source), the whole process will take some time → slower response and then we need to do it all again when recovering for the normal operation

21) CMF applied to a two stage amplifier



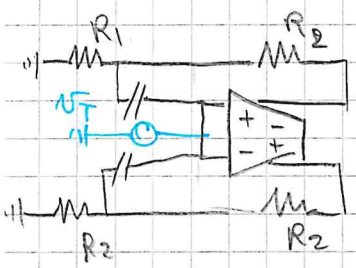
$$\begin{cases} 2I = I_3 + I_4 \\ I_6 + I_7 = I_8 + I_9 \end{cases}$$

Note: V_{IN}^-, V_o^- and V_{IN}^+, V_o^+ are positive!

$$A_{cc} = \frac{V_{o\,cm}}{V_{IN\,cm}} > 0$$

DME: additional offset adjusted by feedback

CME: consider the classic R_1, R_2 feedback:

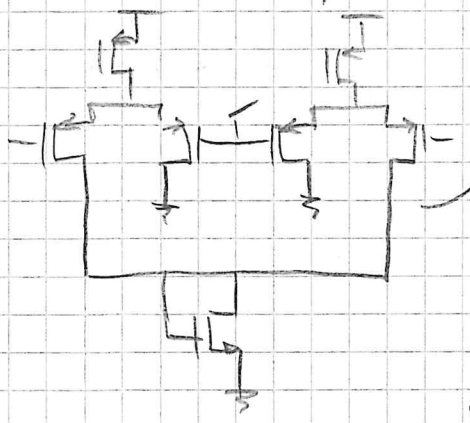


Note that, because of the double inversion, $G_{loop}(0)|_{CM}$ will be positive!

$$G_{loop}(0)|_{CM} = \frac{R_1}{R_1+R_2} \cdot \underbrace{\frac{1}{2r_{o5}}}_{\sim 1} \cdot r_{o3,4}\, \underbrace{g_{m7}(r_{o9} \parallel r_{o7})}_{\text{large}}$$

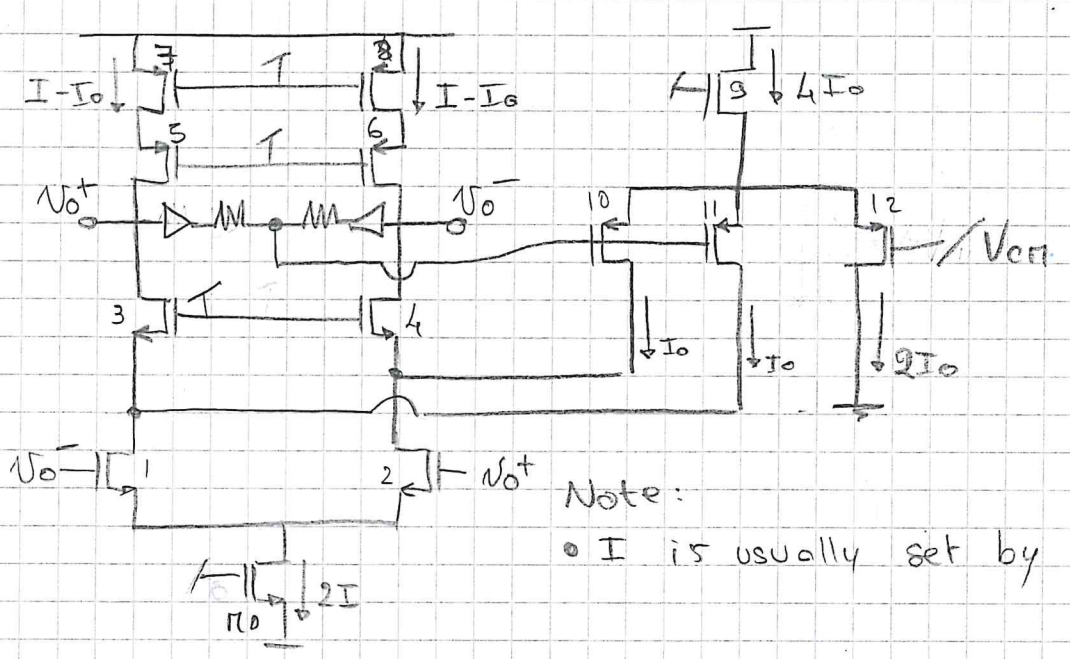
Not CMF!

This loop gain is usually large and wideband. There is no particular solution to this, but since CMF is mandatory, we can:



By picking the other side of the differential pair, we add an extra inversion so that $G_{loop}(0)|_{CMF} < 0$ which is the most important correction to a ΔI in bias conditions

22) CMF applied to a telescopic amplifier



$$\left(\frac{W}{L}\right)_{12} = 2\left(\frac{W}{L}\right)_{10,11}$$

Note:
- I is usually set by SR requirements

Here we're loading the output with a capacitive load and we're directly balancing the bias current instead of going through the tail. Pros/cons:

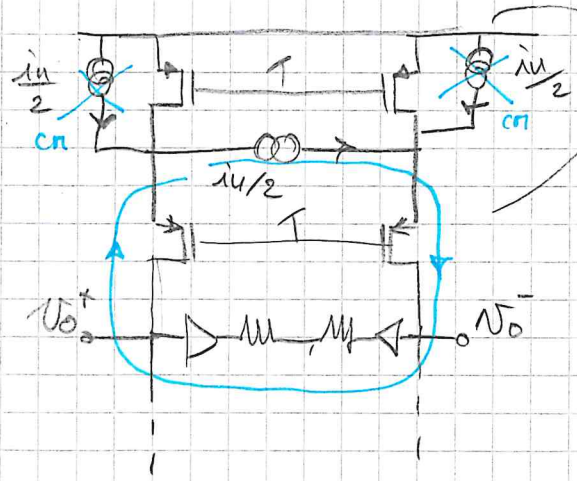
+ faster because $G_{loop}|_{CMF}$ does not go through C_T

− CMF transistors now contribute to $\overline{e_n^2}$. Is it really true

Compute noise contribution:

First of all, M7 and M8 have now lower bias current thus lower noise overall. ($I-I_0$ instead of I).

M7, M8 noise: we split M8 noise in two DM and CM parts (for the justification, see next answer 23)

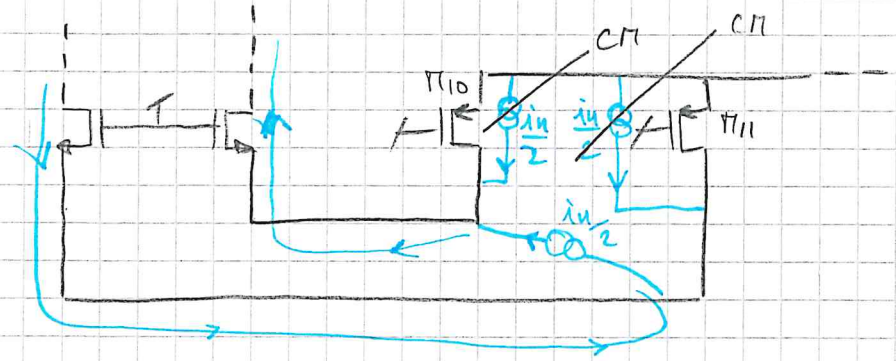


→ CM contribution

$\frac{i_n}{2}$ flows through $V_{OUT_{DIFF}}$, note that noise is lower because of bias current $I-I_0$

$$4kT\gamma g_{m8}\left(\frac{1}{2}\right)^2 = e_n^2\left(\frac{g_{m12}}{2}\right)^2$$

M_{10}, M_{11} DM + CM noise decomposition:



$\frac{i_n}{2}$ of M_{10} flows to the output → $4kTγ g_{m_{10}} \left(\frac{1}{2}\right)^2 = e_n^2 \left(\frac{g_{m_{12}}}{2}\right)$

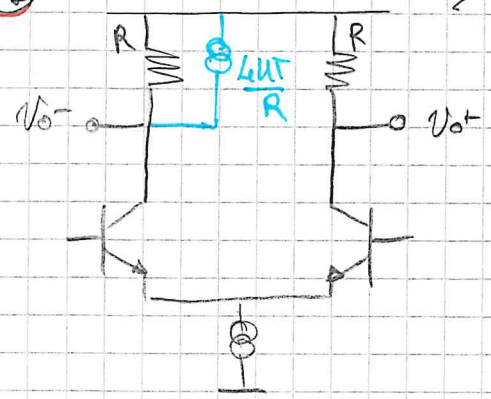
The argument is that CMF lowers mirrors noise by I_0, but at the same time increases stage noise by I_0.

If we carefully select M_{10}, M_{11}, M_{12} V_{OV}, we will end up with a less noisy stage.

However, since there are many close components to place into the layout, this CMF will affect the offset more.

23) Noise CM, DM decomposition, half circuit justification

(1)



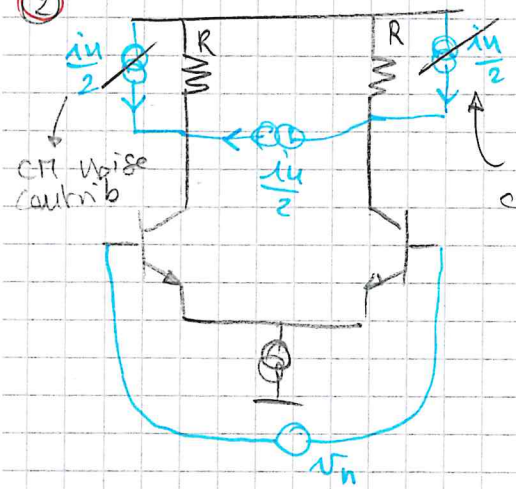
→ What's the differential output noise?

$v_{out}^- = 4kTR \quad v_{out}^+ = 0 \rightarrow v_{DIFF} = 4kTR$

Is it really correct?

Suppose we split $\frac{4kT}{R}$ into two DM, CM contributions:

(2)

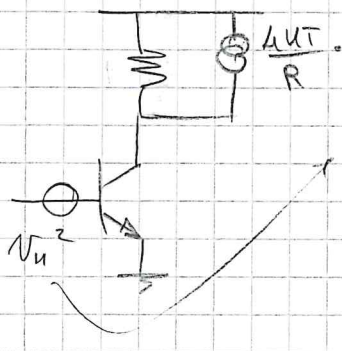


→ Even noise generators are now symmetrical to the central axis, can we do a half circuit noise equivalence?

The 3 current $\frac{i_n}{2}$ generators are totally equivalent to (1)

$$v_{out}|_{DIFF} = \frac{i_n}{2} \cdot 2R \longrightarrow v_n \frac{g_m}{2} \cdot \cancel{2R} = \frac{i_n}{\cancel{2}} \cdot \cancel{2R} \rightarrow \overline{e_n^2} = \frac{4kT}{R} \cdot \frac{1}{g_m^2}$$

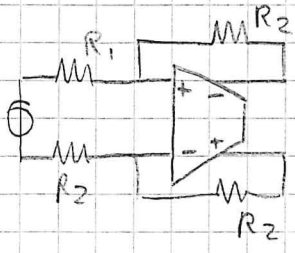
Although being a trivial example, it justifies the use of noise in half circuits:



→ We have two load resistors

$$v_n^2 = 2 \cdot \frac{4kT}{R} \cdot \frac{1}{g_m^2}$$

24) Input / Output common mode voltages with feedback



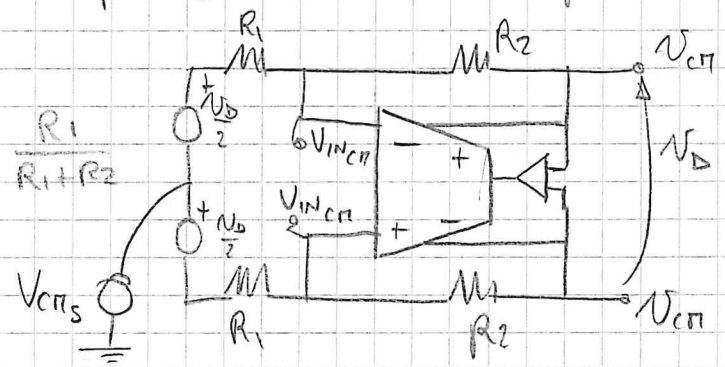
→ This stage cannot be a telescopic amp because the different IN/OUT bias voltages would generate a current in R_1, R_2.
This could be a 2-stage fully diff. amp.

Telescopic amplifiers are used with <u>capacitive feedback</u> most of the times.

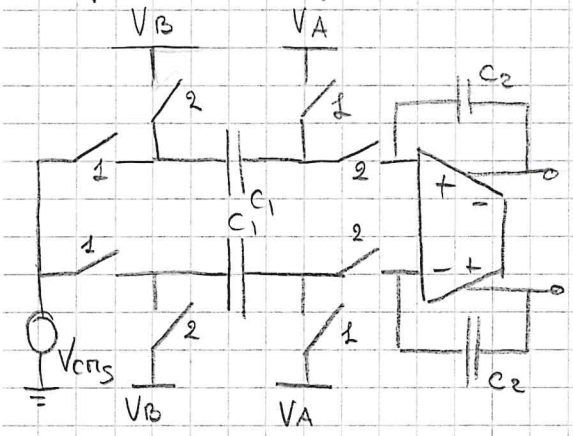
Compute the OTA $V_{CM,IN}$ given input source and output CMF V_{CM} contributions:

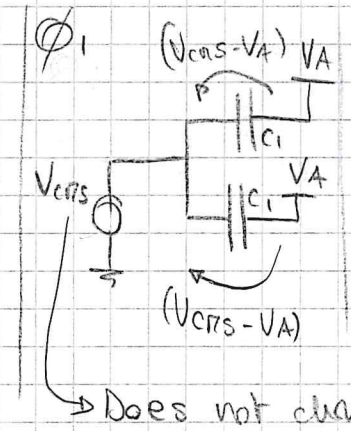
$$V_{IN\,CM}\Big|_{IDEAL} = V_{CM\,SOURCE}\frac{R_2}{R_1+R_2} + V_{CM_0}\frac{R_1}{R_1+R_2}$$

→ $|G_{loop}(0)|_{CMF}| \longrightarrow +\infty$

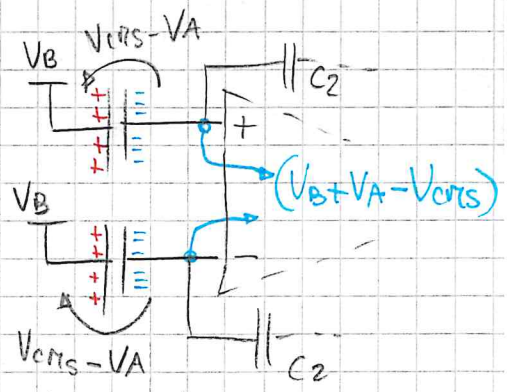


<u>Capacitive feedback</u>: example of a non-inv SW-cap integrator



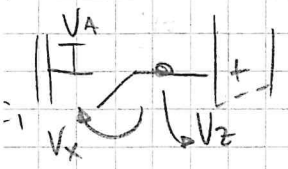


→ Does not change continuously



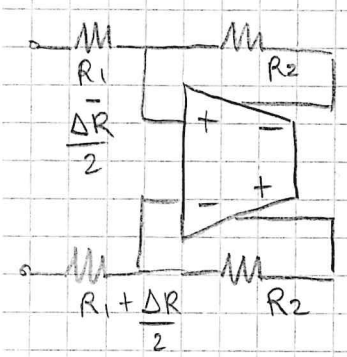
- V_{CM_0} is set by the CMF
- V_{CM_1} is set by V_A, V_B, V_{CMS}
- V_A, V_B need to be chosen based on the SW type (nMOS, pMOS, transmission gate)
- If we have a chain of filters, V_{CMS} will be V_{CM_0} of the previous stage and it will be higher → V_A, V_B set accordingly to $V_{CM\,OUT}$

Practical note:



Be careful with V_Z, we need $V_Z \sim V_A$ so $V_X \sim 0$
This way, we don't have a big V_X onto the SW parasitic capacitor which could inject charges elsewhere thus changing the overall CM dynamics

25) feedback resistors R_1, R_2 mismatch



We can split the mismatch into DIFF/CMF

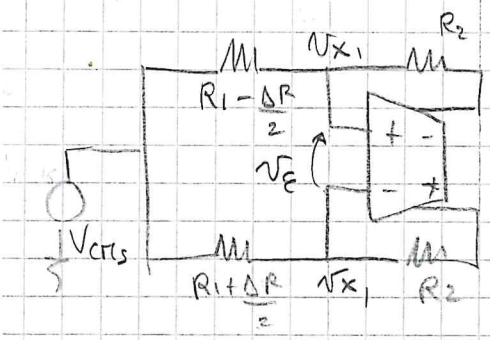
This reasoning is also valid for sw. cap

Assume an ideal OTA, A_{DD} is unchanged:

$$A_{D,D} = \frac{V_D}{R_1 + \frac{\Delta R}{2} + R_1 - \frac{\Delta R}{2}} \cdot 2R_2 = V_D \cdot \frac{R_2}{R_1}$$

If $Gloop_{CMF}(0)$ is not ∞, the ΔR mismatch will introduce an asymmetry $\rightarrow V_{CM\,OUT}$ will be influenced. Moreover

- $A_{D,C}$ will excite $V_{CM\,IN}$ because of the asymmetry
- $A_{C,D}$:



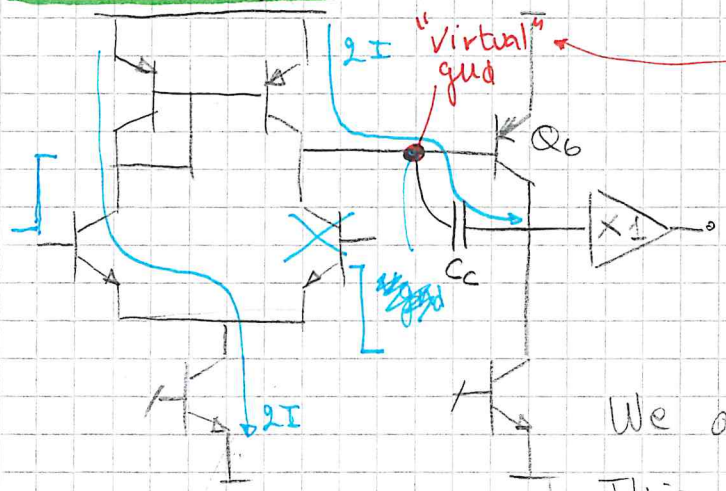
$V_{x_1} = V_{x_2} = V_x$ because $V_\varepsilon \rightarrow 0$

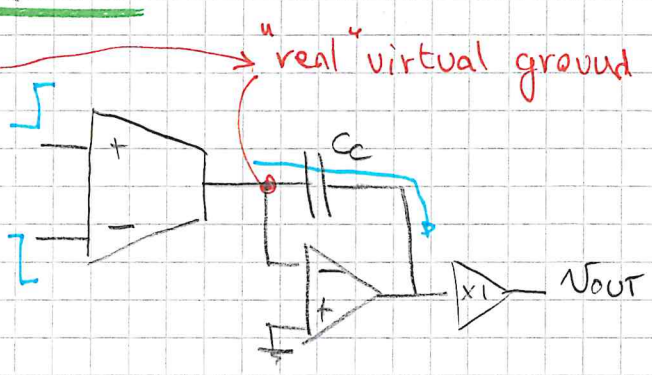
$$\begin{cases} \dfrac{V_x - V_{CMS}}{R_1 - \frac{\Delta R}{2}} = \dfrac{V_1 - V_x}{R_2} \\ \dfrac{V_x - V_{CMS}}{R_1 + \frac{\Delta R}{2}} = \dfrac{V_2 - V_x}{R_2} \end{cases} \rightarrow V_{OUT} = V_1 - V_2 \cong$$

$$V_{OUT} \underset{DIFF}{\cong} V_{CMS}\left(\frac{\Delta R}{R_1 + R_2}\right)\frac{R_2}{R_1}$$

We neglected the $V_{CM\,OUT}$ change but we saw (already knew this result) that $V_{CM} \rightarrow V_{DIFF\,OUT}$

26) Linking GBWP and Slew Rate



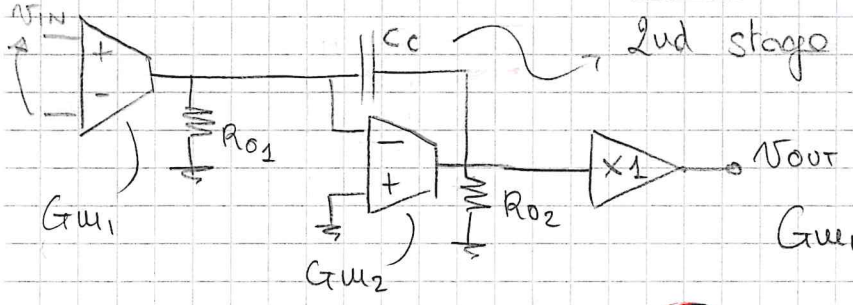


We add C_c on Q_6 for Miller effect

This comes with the positive zero!

Because of r_π, it's difficult to discuss freq response and SR performance. The $\frac{2I}{C_c}$ SR we usually compute can be considered to be "the ultimate" limit. In reality, we make lots of approximations just for ease of computation. Just as an example, we never consider external feedbacks.

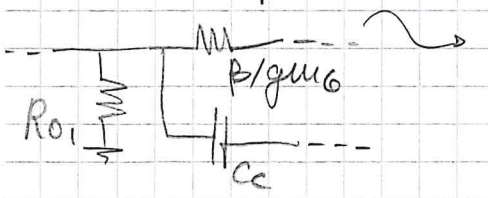
Let's now show that GBWP and SR are tightly related:



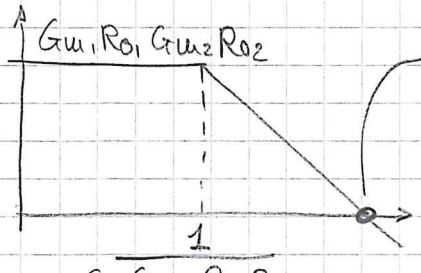
2nd stage with C_c is basically an integrator!

$G_{m1} = g_{m1}$ $G_{m2} = g_{m6}$

Assume $\beta \gg 1$, so:



(1) β/g_{m6} is assumed ∞ so that C_c sees R_{OUT_1} load resistor only



$\omega_0 = \underline{GBWP} = G_{m1}/C_c$ ↝ GBWP cannot be changed too much (let's say one decade is pretty unfeasible) because we didn't consider other singularities.

In general, for a well designed opamp, GBWP is "fixed" by the technology because it's set by HF parasitic capacitances

Better tech → HF poles ↗ ⟹ GBWP can be higher. This is especially true for bipolar because of R_π and higher β (2)

$SR = \frac{2I}{C_c}$ $\quad GBWP = \frac{G_{m1}}{C_c}$ so we can rearrange:

$SR = \frac{2I}{C_c} \cdot \frac{G_{m1}}{G_{m1}} = \frac{2I}{G_{m1}} \omega_u = \frac{2I}{g_{m1}} \omega_u \Rightarrow$ $\boxed{SR = 2 V_{TH} \omega_u}$ Bipolar

GBWP or ω_u

$g_{m1} = \frac{I}{V_{TH}}$

Therefore, for a good bipolar stage, SR and GBWP are linked as computed.

$SR|_{CMOS} = V_{OV} \cdot \omega_u$ ↳ CMOS SR is typ. larger than bipolar ($V_{OV} > 2V_{TH}$)

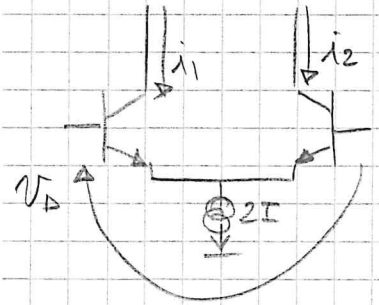
↳ For the same I_{BIAS} it's better to have a smaller g_m:

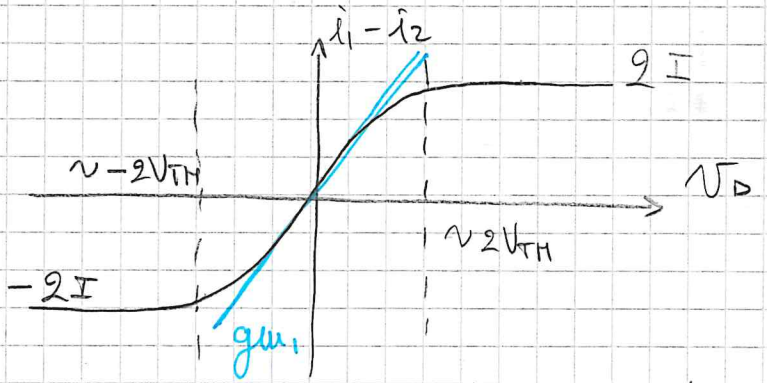
if $g_{m1} \searrow$, $GBWP = \underset{\text{technology}}{\text{constant by}} = \frac{g_{m1}}{C_c}$ so $C_c \searrow \Rightarrow SR = \frac{2I}{C_c} \nearrow$

But remember that lower $g_m \rightarrow$ higher noise and offset!

Note on bipolar diff stage:

When do we reach the completely unbalanced point?



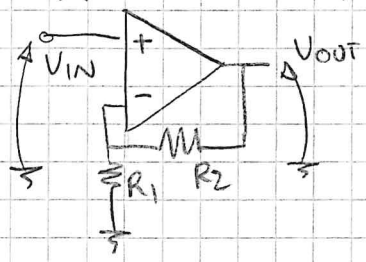


So, saturation point happens when $|v_D| > 2V_{TH} \simeq 50mV$

See what happens during SR in the next page

27) Maximum input sinusoid in a non inverting amplifier

We said that max $|V_D| = 2V_{TH}$ to totally unbalance the differential pair (previous page):



$$\rightarrow SR = 2V_{TH}\omega_0 = 2I/C_c$$

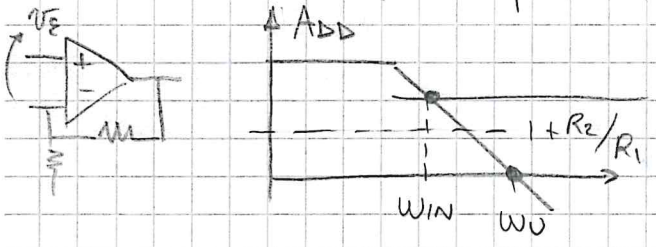
$$V_{OUT}(t) = V_{IN}(t)\left(1+\frac{R_2}{R_1}\right)$$

Apply an input signal $V_{IN} = V_{IN}\sin(\omega_{IN}t)$, then boundary condition is set when max V_{OUT} slope matches SR:

$$\left|\frac{dV_{OUT}}{dt}\right|_{t=0} = V_{IN}\left(1+\frac{R_2}{R_1}\right)\omega_{IN}$$

Then $V_{IN}|_{MAX}\left(1+\frac{R_2}{R_1}\right)\omega_{IN} = 2V_{TH}\omega_0 \rightarrow V_{IN}|_{MAX} = \frac{2V_{TH}\omega_0}{\omega_{IN}\left(1+\frac{R_2}{R_1}\right)}$

We now want to focus at V_ε in this condition:



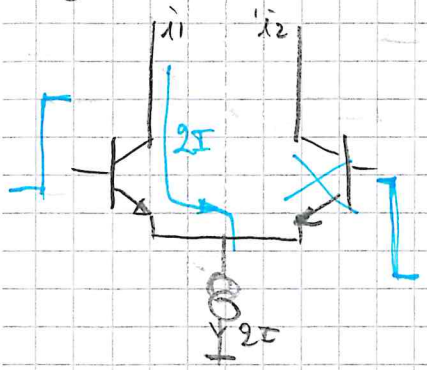
$$A_{DD}|_{\omega=\omega_{IN}} = \frac{\omega_0}{\omega_{IN}}$$

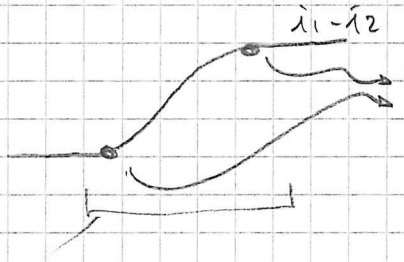
So $|G_{loop}(\omega_{IN})| = -\left(\frac{R_1}{R_1+R_2}\right)\cdot A_{DD}|_{\omega_{IN}} = -\frac{R_1}{R_1+R_2}\cdot\frac{\omega_0}{\omega_{IN}}$ then:

$$V_{\varepsilon\,MAX}\Big|_{\omega=\omega_{IN}} = \frac{V_{IN_{MAX}}}{1+|G_{loop}|} = \frac{2V_{TH}\,\frac{\omega_0}{\omega_{IN}}}{\left(1+\frac{R_2}{R_1}\right)}\cdot\frac{1}{1+\left(\frac{R_1}{R_1+R_2}\right)\cdot\frac{\omega_0}{\omega_{IN}}} \simeq 2V_{TH}$$

neglect

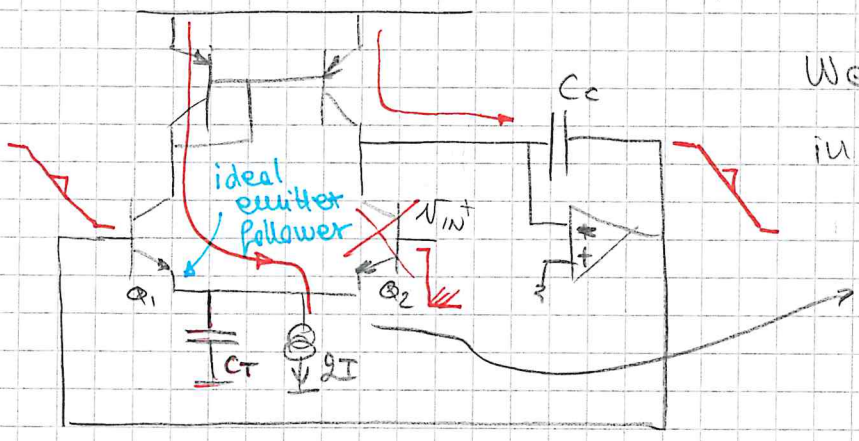
It makes sense, when SR starts to engage, we'd expect V_ε to be at the limit of total unbalance, i.e:



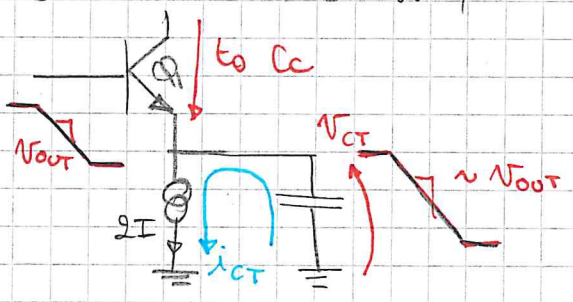


→ So starting from these points $|i_1 - i_2| = 2I$

and $SR = 2V_{TH}\omega_0$



We never consider feedback in SR conditions. Why?



Buffer configuration is the worst.

We apply a large negative step on V_{IN}^+ and instead of $2I/C_C$ we measure a lower SR.

While Q_2 is OFF, Q_1 is ON and on its base V_{OUT} is present. It is immediate to see that Q_1 and $2I$ form an ideal emitter follower, therefore $V_B|_{Q_1} = V_E|_{Q_1}$

However, C_T is also present and i_{CT} is the discharge current because $V_{CT} \cong V_{OUT}$! So:

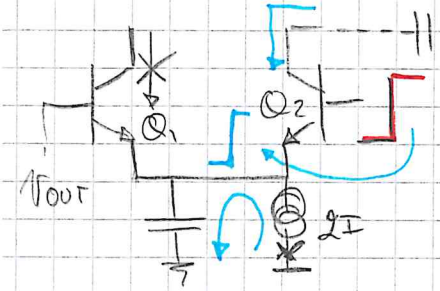
$$|SR_{Real}| = \frac{2I}{C_C + C_T} = \frac{2I}{C_C} \cdot \frac{1}{1 + \frac{C_T}{C_C}}$$

↳ Worsening factor due to C_T

Modern technology reduced C_T value, but this is just an example that shows SR is more complicated than it looks

If we instead use a R_1, R_2 feedback, C_T sees a smaller voltage thus discharges at a lower rate

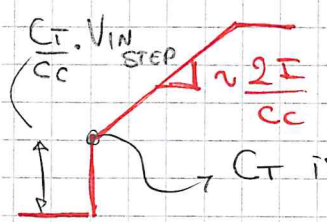
Furthermore, this feedback is not symmetrical!



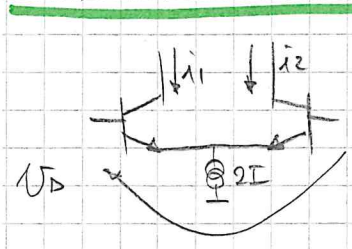
Now Q_2 is an ideal emitter follower

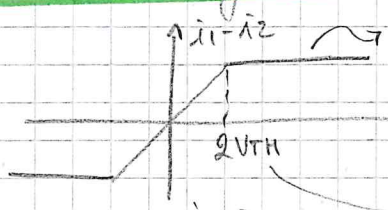
Step on $V_B|_{Q_2}$ → Step on $V_e|_{Q_2} = V_{CT}$

A voltage step on C_T means that we need to charge C_T with an instant current coming from the second stage → V_{OUT} step



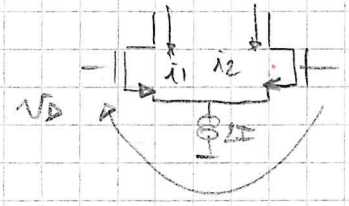
29) SR increase with degeneration

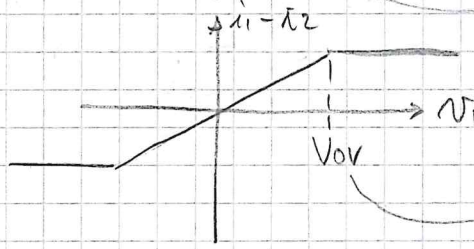




SR because one transistor is killed

$$SR\big|_{bip} \cong 2V_{TH} \cdot \omega_u$$



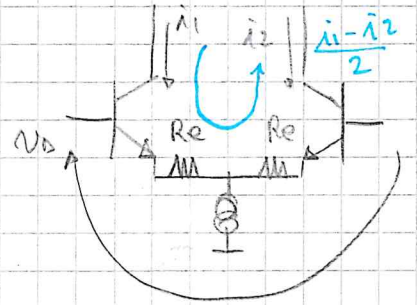


$$SR\big|_{CMOS} \cong V_{ov} \cdot \omega_u$$

We intuitively get that by extending the linear range we increase SR performance:

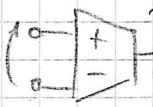
- Slope in $v_D = 0$ is g_m → reduced gain
- Higher noise and offset because of lower $i_D = \frac{g_{m1,2}}{2} v_D$
- If in CMOS we V_{ov} ↗ ⇒ we pay in terms of CM voltage dynamics of input and output

Increase SR in bipolar opamps → degenerate



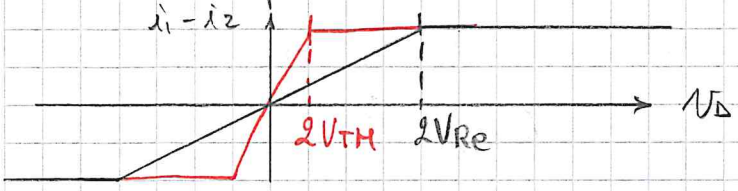
$$\frac{i_1 - i_2}{2} = \frac{v_D}{2 + 2R_e g_m} \approx v_D / 2R_e$$

↳ good degeneration $g_m R_e \gg 1$

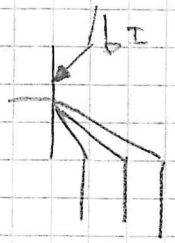
It follows that  $G_{m1} = \frac{1}{R_e}$

$$SR = \frac{2I}{C_c} \quad \omega_u = \frac{G_{m1}}{C_c} = \frac{1}{R_e C_c} \Rightarrow \underline{SR = 2I R_e \omega_u}$$

We end up with a $2V_{Re}$ contribution instead of $2V_{TH}$:

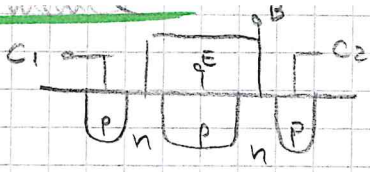


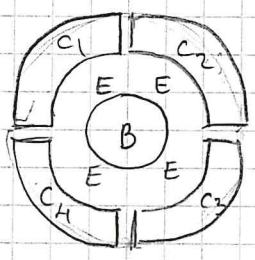
Since it's possible to design the stage so that $V_{Re} \gg V_{TH}$, SR will increase a lot but at the same time it will perform badly in terms of noise / offset, CM voltage dynamics, ---



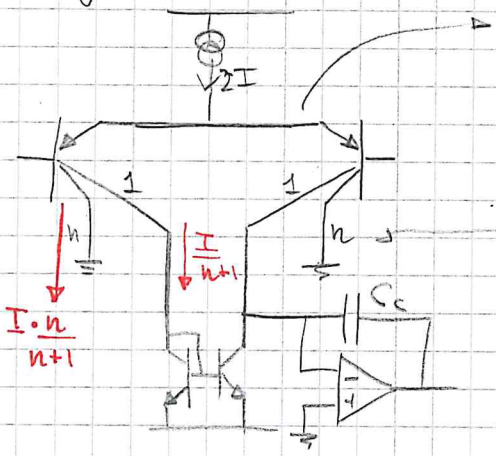
Multicollectors are easy to make in lateral pnps (not really feasible for npn vertical transistors)

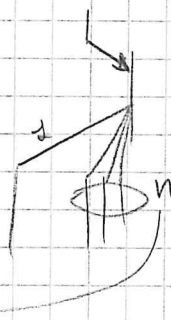
With npn it's easy to make multiemitters





How can we use it? It was used as an old design trick:





grouped collectors

By wasting $I \cdot \frac{n}{n+1}$ current, it's like having an equivalent stage with I/n bias

Issues at the time (around 1970s):

- Cc was larger than the opamp itself (too much area)
- 2I can't be reduced because, being already at the limit, β would start to drop

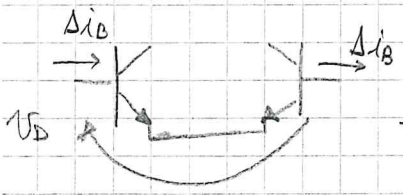
By wasting current we get: $\omega_u = \frac{G_m}{C_c}$ where $G_m = \frac{g_m}{n+1}$

- G_m is reduced → SR is also reduced $\left(SR = \frac{2I}{(n+1)C_c}\right)$
- We can decrease Cc value so that G_m and SR are the same with a <u>lower capacitor area</u>.

The LM741 uses another multicollector type of circuit to also decreasing Cc value but with keeping a reasonable SR performance.

$SR = 2 \cdot (n+1) V_{TH} C_c$ Since we have a n+1 multiplying factor, we can relax the capacitor requirement to get the same SR and ω_u of before but with a smaller Cc area

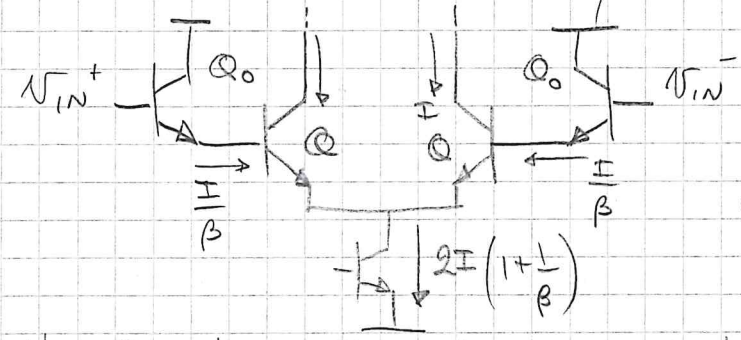
31) Input impedance of a diff pair



$$\frac{v_D}{\Delta i_B} = z_{IN}\Big|_{DIFF} = 2 r_\pi = 2\frac{\beta}{g_m}$$

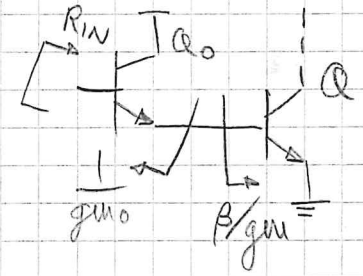
To increase z_{IN} we can decrease I_{BIAS} so that $\frac{1}{g_m}$ increases → be careful of β drop

We can increase z_{IN} by adding another pair:



Note:
- I of Q is already low
- I of Q_0 will make β of Q_0 drop for sure → $\beta|_{Q_0} \simeq \frac{1}{3}\beta|_Q$

Let's see how z_{IN} is increased. Half circuit:



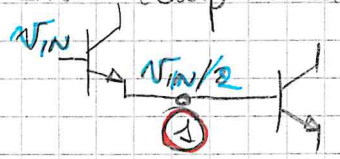
$$R_{IN} = \beta_0\left[\frac{1}{g_{m_0}} + \frac{\beta}{g_m}\right]$$ trivial to see $\frac{1}{g_{m_0}} \simeq \frac{\beta}{g_m}$

$$R_{IN} \simeq \beta_0\left[2\frac{\beta}{g_m}\right]_{I=10\mu A}$$ → $R_{IN} \sim$ 100s of MΩ

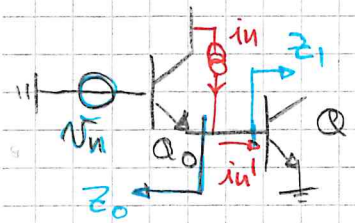
($\beta_0 \approx 80$, $\frac{\beta}{g_m} \approx 250$)

This R_{IN} must be multiplied by 2 because of the other half

Issues:
- β_0 is not good
- low $I_{C_{Q_0}}$ leads to low f_T → low speed. It can be ok for LF applications (e.g. INA temp. measure)
- Half gain because $\frac{1}{g_{m_0}} = \frac{\beta}{g_m}$:



- Low current → high noise!



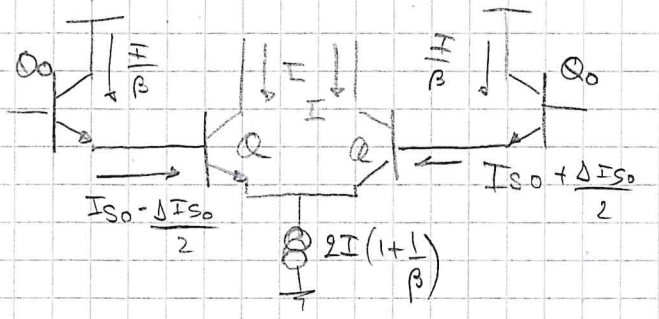
$$i_n' = i_n\frac{z_0}{z_0+z_1} = \frac{v_n}{z_0+z_1}$$

$$\overline{E_n^2} = \frac{2qI_{C_0}}{g_{m_0}^2} = 2V_{TH}\frac{1}{g_{m_0}}$$

$$\overline{E_n^2} = \underbrace{2\cdot\left(2V_{TH}\frac{1}{g_{m_0}}\right)}_{Q_0} + \underbrace{2\left(2V_{TH}\frac{1}{g_m}\cdot 4\right)}_{Q}$$ Because of ①

→ This term will be dominant because $\frac{1}{g_{m_0}} = \beta\frac{1}{g_m}$

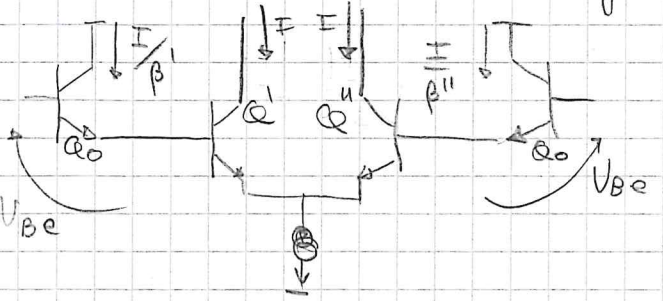
Offset contribution



Consider a I_S mismatch on Q_0 transistors:

$$V_{OS}\Big|_{I_{S0}} \simeq V_{TH}\,\frac{\Delta I_{S0}}{I_{S0}}$$

We also have a not negligible contribution of β mismatch:

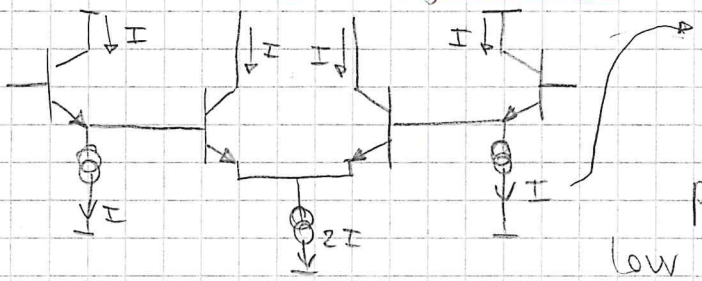


We get a V_{BE} mismatch because of β and so:

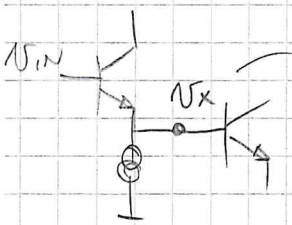
$$V_{OS}\Big|_{\beta} \simeq V_{TH}\,\frac{\Delta\beta}{\beta}$$

Calculations are standard, it's just to highlight some issues.

Enhancement using ideal emitter followers



Current generators will have the same I_{BIAS} of the diff pair because current is already low and β should/it drop so much.



$$V_X = V_{IN}\cdot\frac{\beta/g_m}{\frac{1}{g_{m0}}+\beta/g_m} \overset{(1)}{=} V_{IN}\,\frac{\beta}{\beta+1} \simeq V_{IN}$$

↳ "ideal" follower

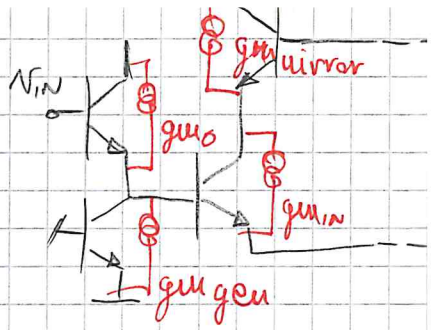
(2) $I_{Q0} = I_Q \rightarrow g_{m0} = g_m$

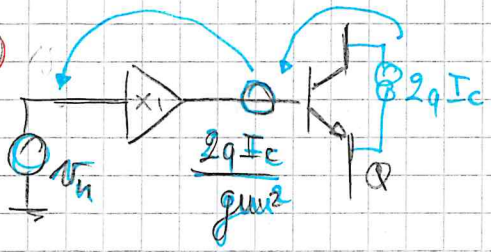
$R_{IN} \simeq \beta\left[\beta\cdot\frac{1}{g_m}\right]$ ↝ should be 2/3 times higher than before because β_0 does not drop anymore

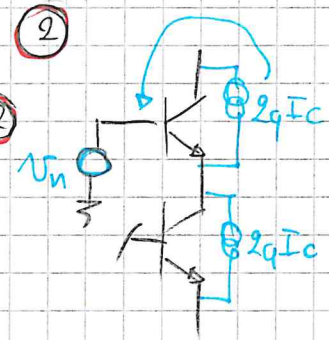
Issue = double the burned power because of the additional current generators

Stage noise : consider just I_C

$$\overline{E_n^2} = 2\left[\underbrace{\frac{2qI_C}{g_{m_{IN}}^2} + \frac{2qI_C}{g_{m_{MIRROR}}^2}}_{①} + \underbrace{\frac{2qI_C}{g_{m_O}^2} + \frac{2qI_C}{g_{m_{gen}}^2}}_{②}\right]$$

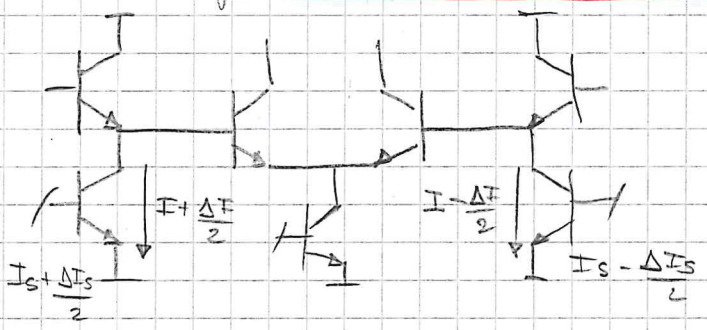


① 

② 

Power is doubled but noise is way better than before (doubled noise instead of $\sim\beta_0$ times)

Current generator mismatch

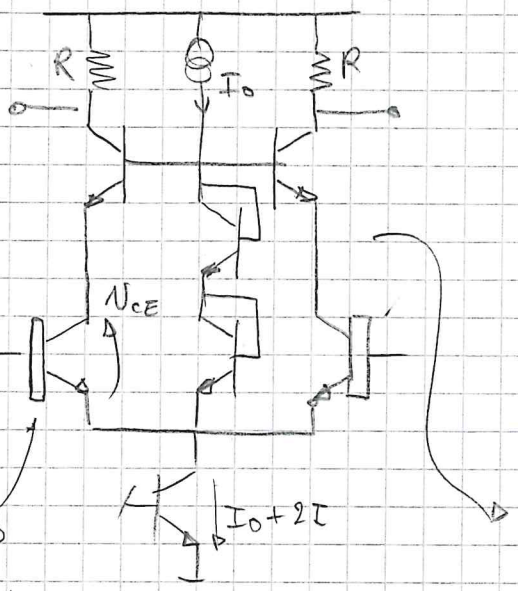


If current generators have ΔI_S mismatch, by doing the same old math we end up with

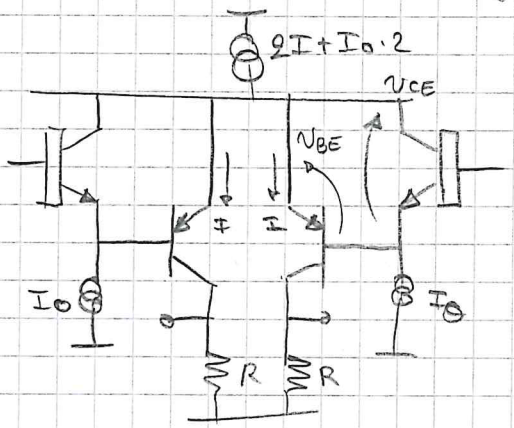
$$V_{OS} \simeq V_{TH}\frac{\Delta I_S}{I_S}$$ because $\Delta I_S \to \Delta I$

32) Super β transistors

By designing very thin base width we can achieve high current gain ($\beta \sim 1000s$). However, this comes at a cost: diffusion between collector and emitter can penetrate enough if V_{CE} is too high ⇒ Breakdown voltage ($V_{CE_{MAX}}$) of super β transistors is unusually low ($\sim 5V$) → We need to desig circuits that limit V_{CE} swings:



Super β symbol

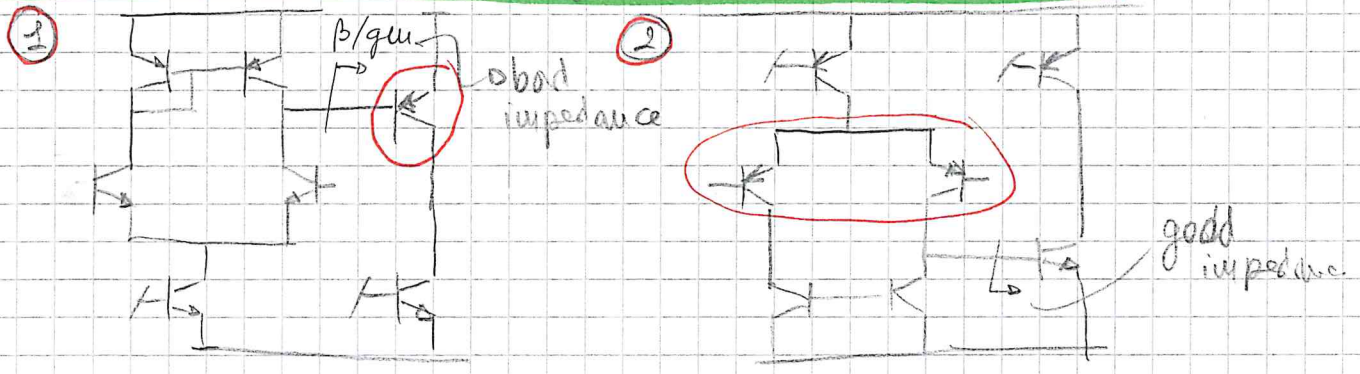


Super β $V_{CE} \simeq V_{BE_{pnp}}$

Cascode limits the V_{CE} of Super β

We need to devise different topologies that limit the super β breakdown voltage

32) LM741: level shifting issue and new idea

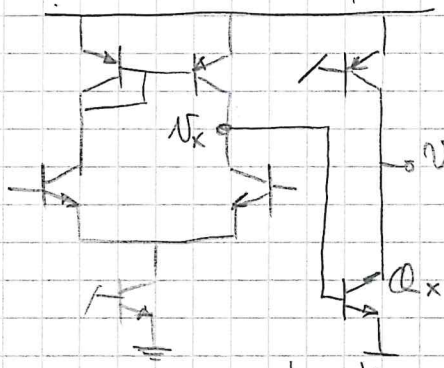


Issues:

① 2nd stage has low β and pnp is slower. Low β means R_{OUT_2} ↘

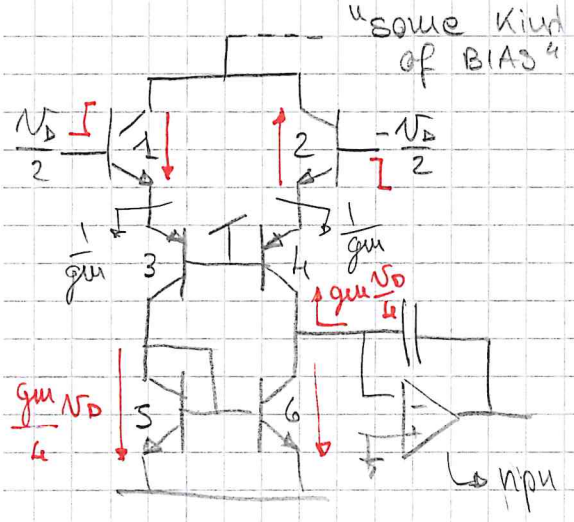
② 1st stage has pnp transistors → still bad

Can we think of a solution? npn first stage + npn 2nd stage:

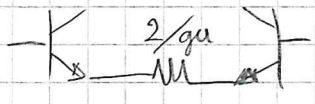


↳ <u>level shifting issue</u>: $V_{BE\,Qx} \sim 0{,}7$ but V_x is way above gnd. We could place a V_B source instead but this would mean reducing V_{out} swing by a lot.

Let's see how LM741 goes around this:

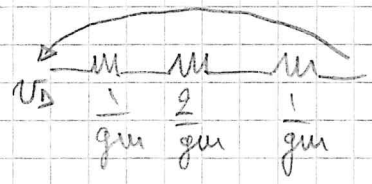


Q_1, Q_2 emitters are degenerated by the very same $\frac{1}{g_m}$ → small degeneration (it will be used for biasing the stage)



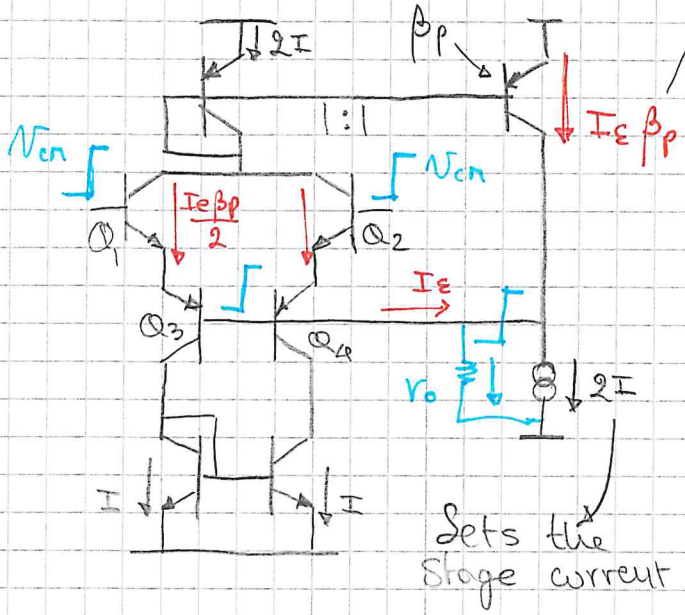
$g_m R_e = g_m \cdot \frac{1}{g_m} = 1$

↳ local Gloop

Because of  → $I_D = V_D / \left(4 \cdot \frac{1}{g_m}\right)$

Q_3, Q_4 are used for biasing (see later) and level shifting. Since they are cascodes, they do not introduce speed / low β issues!

LM741 first stage biasing



β of the pnp transistor increases the loop gain.

$I\varepsilon\,(1+\beta_p) = 2I$

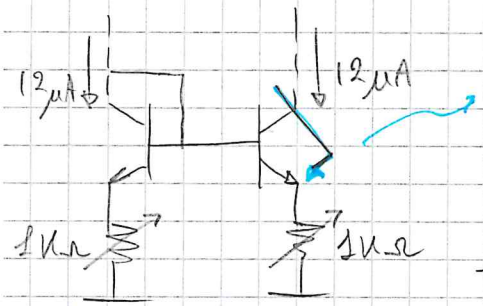
$I\varepsilon = \frac{2I}{1+\beta_p}$

↳ error signal

We see that $G_{loop}(0) = -\beta_p$

What's $A_{c,c}$? See blue lines: a V_{cm} input increases the base of Q_3, Q_4, the current increase will be set by the r_o of the 2I current generator

Mirror degeneration



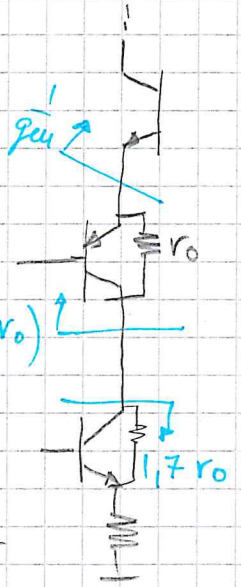
Input bias current is 12μA → $\frac{1}{g_m} = 2{,}5k\Omega$

$R_{coll} \to \infty$ if $g_m R \gg 1$

But $R \sim 1k\Omega$ so $\frac{1k}{2{,}5k}$ is not $\gg 1$

The degenerating resistors are in fact used for offset correction (they're variable), not for increasing the collector resistance. To first order, we can consider the stage to be NOT degenerated (when computing noise and Rc).

$A_{D,D}\big|_{\substack{w/o\\ 2nd\\ stage}} = \frac{g_m}{4} \cdot 2\,R_{OUT}$ ↝ R_{OUT} is very difficult to evaluate because of feedback



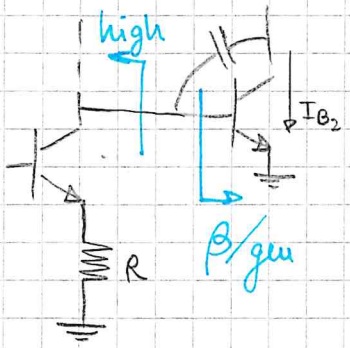
where $R_{OUT} = 2r_o \,//\, 1{,}7\,r_o \cong r_o$

approx ($(\frac{1}{g_m} g_m r_o + r_o) \sim 2r_o$

The feedback bias network will increase the equivalent resistance up to few ~MΩ (not shown)

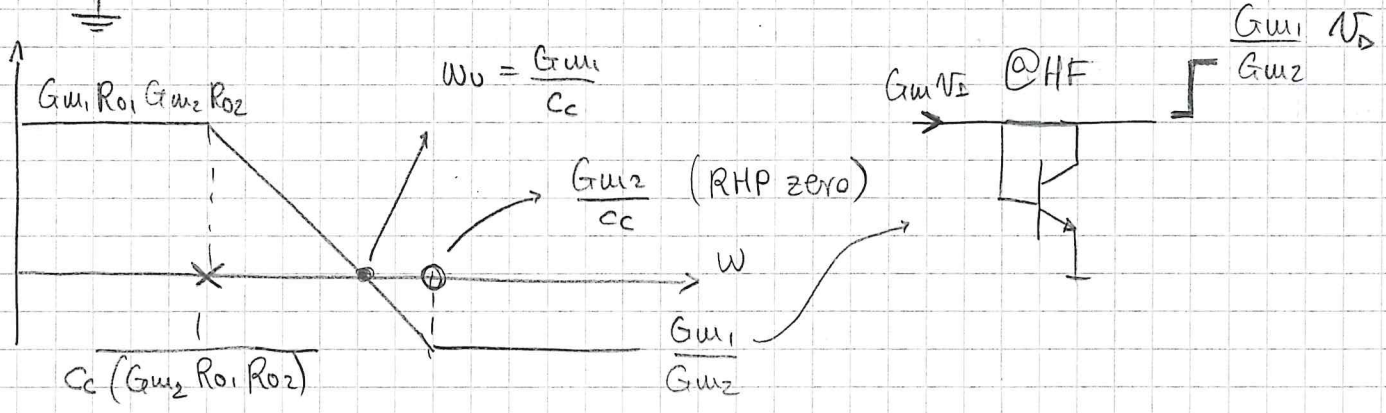
Frequency response

For R_{OUT} we did not consider the 2nd stage:



β/g_m is fairly low wrt R_{OUT_1}

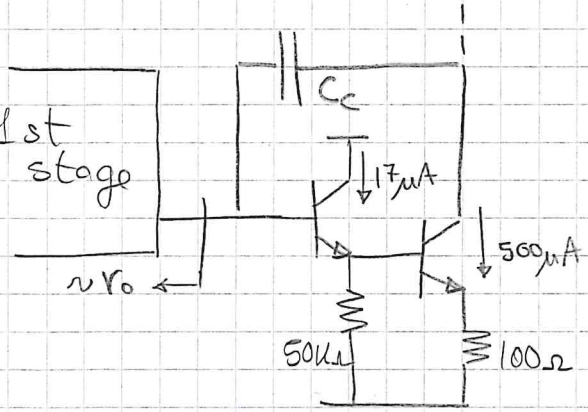
Reason: $I_{BIAS\ 2nd\ stage}$ is high because of frequency compensation, so $\frac{1}{g_m}$ is low-



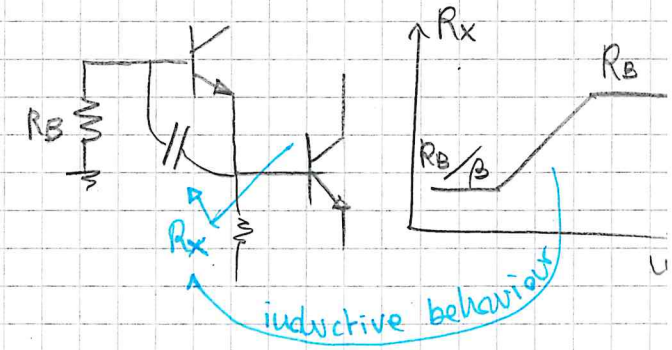
To move the RHP zero away from the pole → G_{m_2} ↗↗ so I_{BIAS_2} needs to be large.

Note: in CMOS we use the nulling resistor because increasing 2nd stage bias current would lead to a large V_{OU} → this would lead to systematic offset on the first stage and it needs to be avoided by design (see analog circuit design notes!)

What can we do to increase β/g_m seen resistance? Buffer

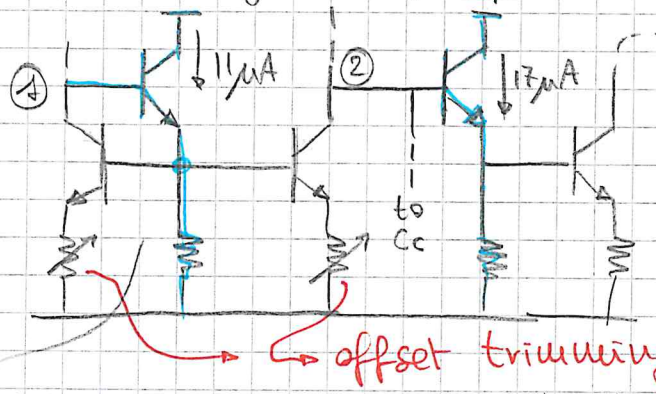


HF →



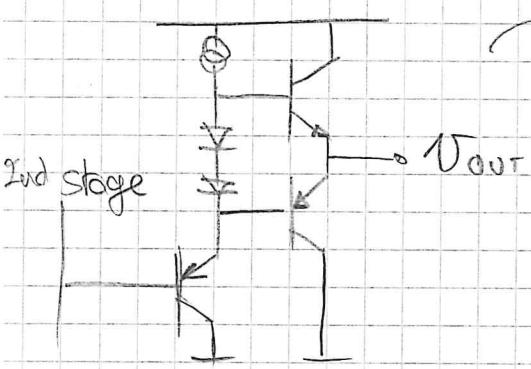
Darlington pair increases DC resistance, however it shows an inductive behaviour! → Frequency compensation (together with C_c) is a mess → Bipolar are difficult to use because of R_π

Compensating the β problem



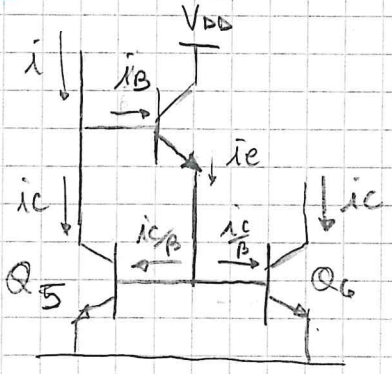
↳ There are some similarities on nodes ① and ② thanks the the β comp generator and to the darlington generator. Bias currents (11μA and 17μA) are probably different because there can be some room for offset trimming through R

Output stage of the LM741



↳ Shown but not analyzed

Input stage mirror β-helper circuit calculation



$V_{BE_5} = V_{BE_6}$, suppose $I_{S5} = I_{S6}$, then

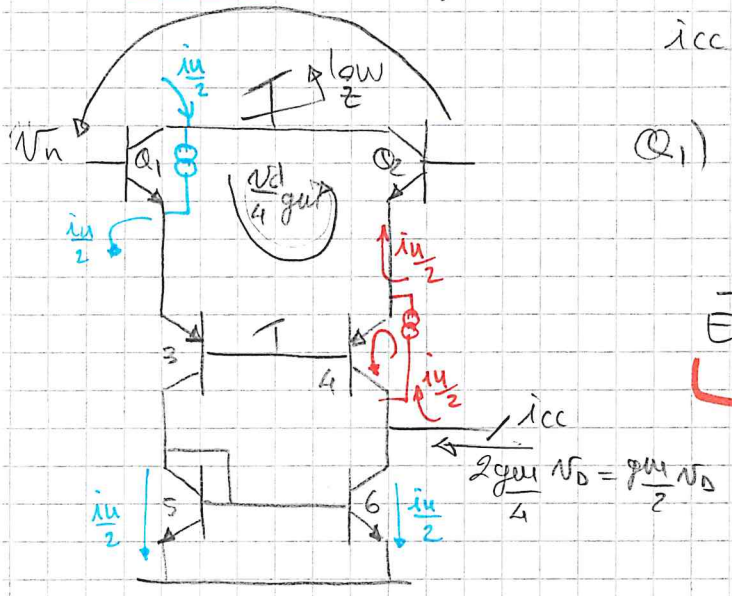
$$V_{TH}\ln\left(\frac{I_{C5}}{I_{S5}}\right) = V_{TH}\ln\left(\frac{I_{C6}}{I_{S6}}\right) \rightarrow I_{C5} = I_{C6} = i_c$$

$$i = i_c + i_B = i_c + \frac{i_e}{\beta+1} = i_c + \frac{i_c}{\beta+1}\left(\frac{1}{\beta} + \frac{1}{\beta}\right)$$

$$i = i_c\left(1 - \frac{2}{\beta(\beta+1)}\right)$$

So we get a β enhancement on the $i - i_c$ difference (remember, for a 1:1 mirror $i_{IN} = i_{OUT} \rightarrow i = i_c$ ideally)

LM741 input stage noise



$$i_{cc}\big|_{v_n} = 2 \cdot \frac{g_m}{4} v_n = \frac{g_m}{2} v_n$$

Q_1) $v_n \cdot \frac{g_m}{2} = \frac{i_u}{2}$ ↳ i_u divides by half because of the degeneration

$$\overline{E_{u\,1+2}^2} = \frac{2qI_c}{g_m^2} \times 2$$

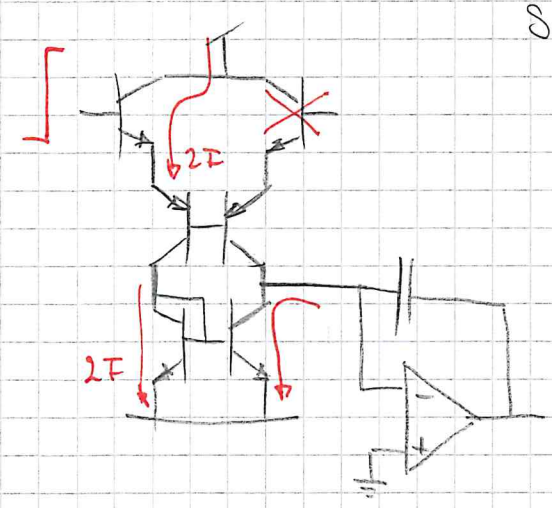
Q_3, Q_4) Same Q_1, Q_2 contribution

Q_5, Q_6) Directly flows through the out → ① → $\overline{E_{u\,5+6}^2} = \frac{2qI_c}{g_m^2} \cdot 4 \times 2$

$$\overline{E_{u\,TOT}^2} = 12 \times \frac{2qI_c}{g_m^2}, \text{ if } I_c \sim 10\mu A \rightarrow \overline{E_{u\,TOT}^2} = 200\,n\frac{V^2}{Hz} = \left(14{,}4\,\frac{nV}{\sqrt{Hz}}\right)$$

If we consider V_{DD} noise $\overline{E_{u\,TOT}^2} \sim \left(17\,\frac{nV}{\sqrt{Hz}}\right)^2$, if we consider the variable resistors → $\overline{E_{u\,TOT}^2} \sim \left(16\,\frac{nV}{\sqrt{Hz}}\right)^2$ ↳ noise is slightly lower thanks to the mild degeneration of the mirror!

LM741 Slew Rate



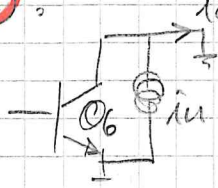
$$SR = \frac{2I}{C_c} \qquad \omega_U = \frac{g_m/2}{C_c}$$

↳ general purpose opamps are unconditionally stable!

$$SR = \frac{2I\omega_U}{\frac{g_m}{2}} = 4\,V_{TH}\,\omega_U$$

↳ 2 for the standard opamp

①:

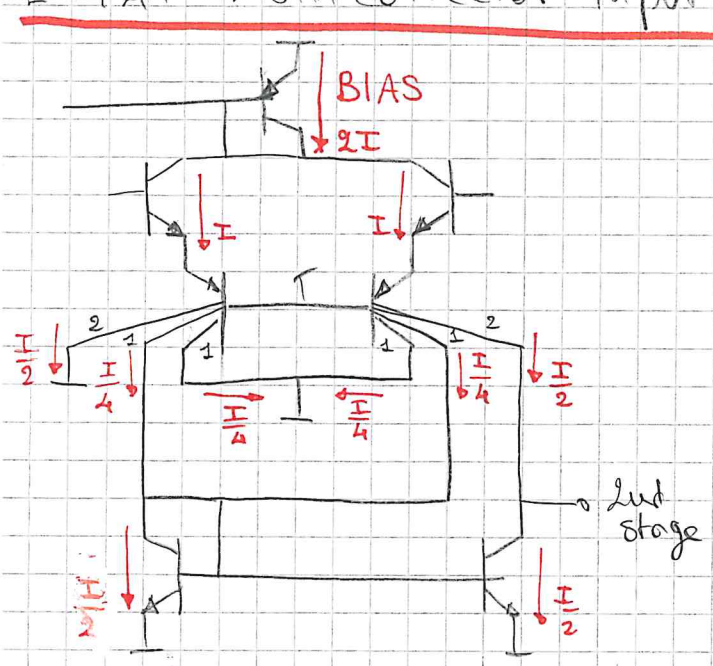


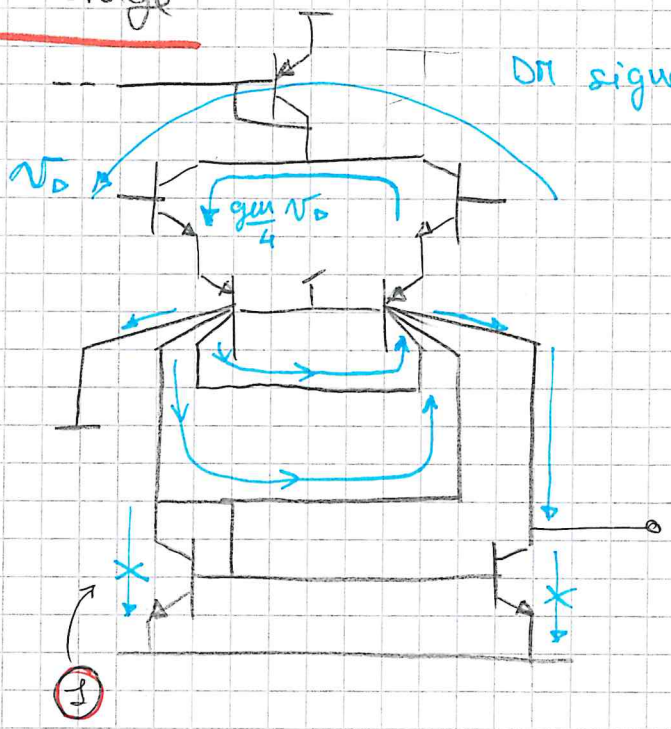
$$i_{cc} = i_u = \frac{g_m}{2} v_{n\,IN} \rightarrow \overline{v_{u\,IN}^2} = \frac{4}{g_m^2} \cdot 2qI_c = \overline{E_{n\,5,6}^2}$$

because of the lower input G_m, it goes by itself that mirror noise is amplified (see exam example 10, the same thing happens)

So $\overline{E_{u\,TOT}^2} = (2 + 2 + 4 + 4) \times \frac{2qI}{g_m^2}$ ↳ Mirror Q_5, Q_6 are 4 times noisier than Q_1, Q_2. ...

LM741 Multicollector input stage

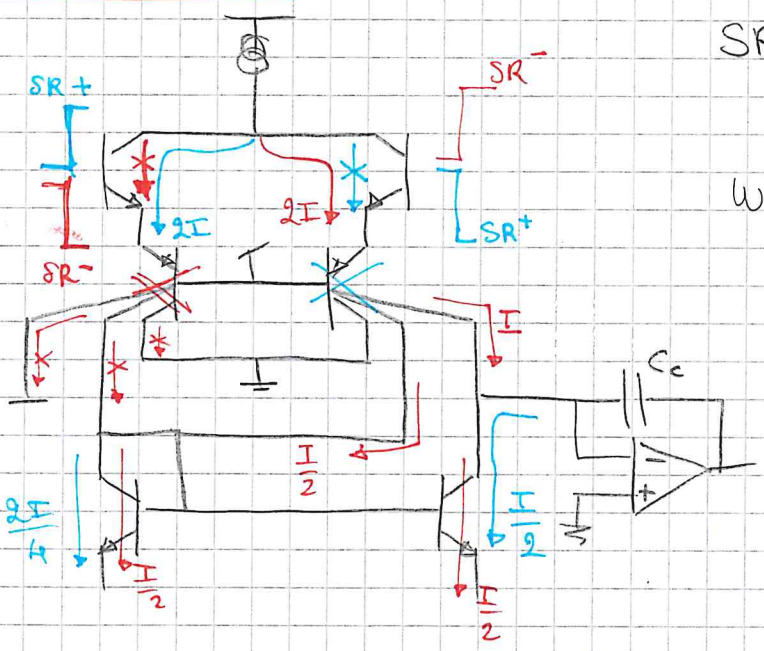




Multicollector was used to reduce C_c size.

(2) In DM, mirror current is zero! Why, because of bias, CMRR, etc... reasons, so it doesn't double in current as usual.

Slew rate:



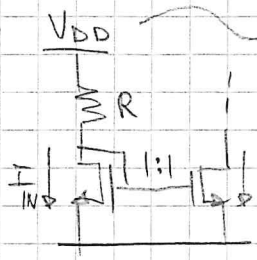
$$SR^{\pm} = \frac{I}{2}\frac{1}{C_c}$$

$$\omega_U = \frac{G_m}{C_c} = \frac{g_m}{8C_c}$$

$$\rightarrow SR = 4 V_{TH}\,\omega_U$$

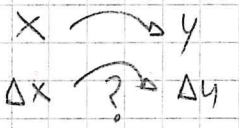
Slew Rate is the same of the non-multicollector version, but here C_c area is smaller!

33) Simple current refereuce and sensitivity of a parameter



How does I_{IN} value changes with V_{DD}? V_{DD} can be regulated (zener, etc---) but we'd like something <u>insensitive</u> to disturbs

$I_{IN} = I_{OUT}$ $\quad I_{IN} = \frac{V_{CC} - V_{BE}}{R}$ ↳ for bipolar



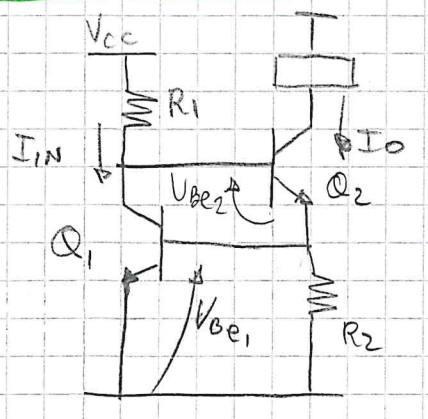
How do we estimate the relative change of a quantity Δy given Δx?

<u>Def</u> Sensitivity $S_x^y = \frac{\Delta y / y}{\Delta x / x} \cong \frac{\partial y}{\partial x} \frac{x}{y}$ (small changes) In our case:

$$S_{V_{CC}}^{I_o} = \frac{V_{CC}}{I_o} \frac{\partial I_o}{\partial V_{CC}} = \frac{V_{CC}}{\frac{V_{CC} - V_{BE}}{R}} \cdot \frac{1}{R} = \frac{V_{CC}}{V_{CC} - V_{BE}} \rightsquigarrow > 1$$

If $V_{CC} >> V_{BE}$ then $S_{V_{CC}}^{I_o} \approx 1$

34) V_{BE} current reference



Important: always check loop gain ①

$$I_{IN} = \frac{V_{CC} - 0,7 - 2}{R_1} \qquad I_O = \frac{V_{BE1}}{R_2}$$

V_{BE_1} does not change much with I_{IN}, so sensitivity is way flatter than before

Note: I_B is neglected

$$S_{V_{CC}}^{I_O} = \frac{V_{CC}}{I_O}\frac{\partial I_O}{\partial V_{CC}} \qquad V_{BE1} = V_{TH}\ln\left(\frac{I_{IN}}{I_{S1}}\right) \longrightarrow I_O = \frac{V_{TH}\ln\left[\frac{I_{IN}}{I_{S1}}\right]}{R_2}$$

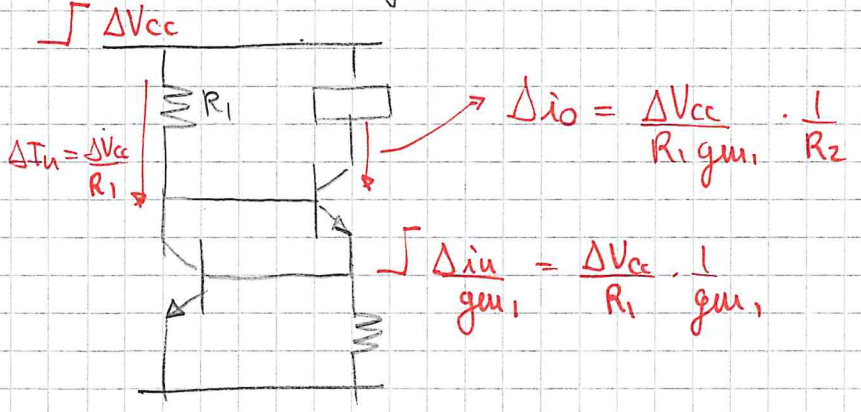
$$= \frac{V_{CC}}{I_O}\frac{V_{TH}}{R_2}\cdot\frac{1}{\frac{I_{IN}}{I_{S1}}}\cdot\frac{1}{I_{S1}}\frac{\partial I_{IN}}{\partial V_{CC}} = \frac{V_{TH}}{V_{BE1}}\left[\frac{V_{CC}}{I_{IN}}\frac{\partial I_{IN}}{\partial V_{CC}}\right] = \underbrace{\frac{V_{TH}}{V_{BE1}}}_{\text{improvement factor}} S_{V_{CC}}^{I_{IN}}$$

(V_{BE_1})

- $S_{V_{CC}}^{I_{IN}} \simeq 1$, $V_{TH} \sim 25mV$, $V_{BE} \sim 0,7$ $\Big]\rightarrow S_{V_{CC}}^{I_O} = 0,037$ so

for a ΔV_{CC} % $\Big]\longrightarrow \frac{\Delta I_{IN}}{I_{IN}} \sim 10\%$ while $\frac{\Delta I_O}{I_O} \sim 0,37\%$

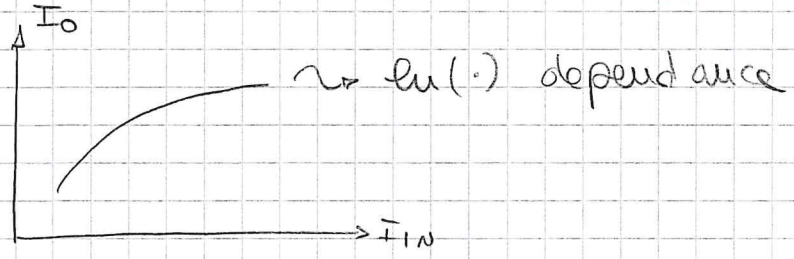
Since we're using derivatives, we can find the same result by:



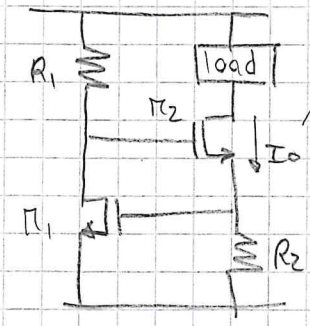
look at ①

$$S_{V_{CC}}^{I_O} = \frac{V_{CC}}{I_O}\frac{\Delta I_O}{\Delta V_{CC}} = \frac{V_{CC}}{I_O}\frac{1}{R_2 g_{m_1} R_1} = \frac{V_{TH}}{V_{BE1}}\left[\frac{V_{CC}}{I_{IN}}\cdot\frac{1}{R_1}\right] = \frac{V_{TH}}{V_{BE1}} S_{V_{CC}}^{I_{IN}}$$

(V_{BE_1}; $g_{m_1} R_1 = I_{IN}/V_{TH}$)



35) CMOS version of the Vbe current ref



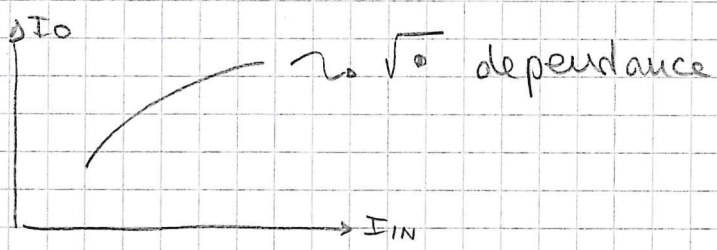
→ Sensitivity is higher wrt bipolar because ln[ ] is flatter than sqrt( )

$$I_O = \frac{V_{GS1}}{R_2} = \frac{V_{T1} + \sqrt{\frac{2I_{IN}}{(\frac{W}{L})_1 \mu C_{ox}}}}{R_2} \xrightarrow{(\frac{W}{L})\gg 1} \frac{V_T}{R_2}$$

Math is the same as before:

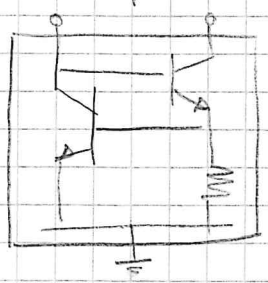
$$S_{VDD}^{I_O} = S_{VDD}^{I_{IN}} \frac{V_{OV1}/2}{V_{GS1}}$$

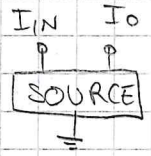
Issues: we did not consider: temperature, mismatches, r_o, Z_{OUT} of the reference, load change, ---

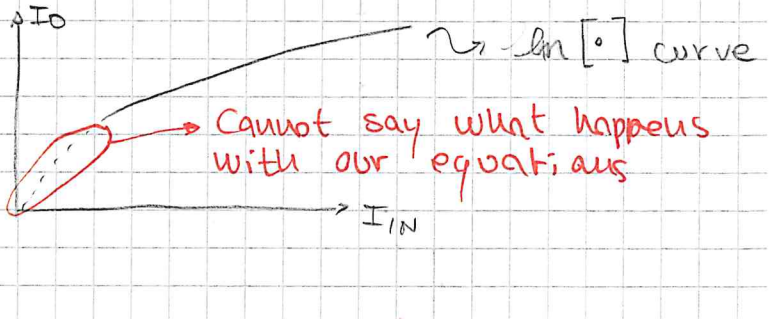


36) Bootstrap and positive feedback on current ref

Let's find a way to achieve lower sensitivity



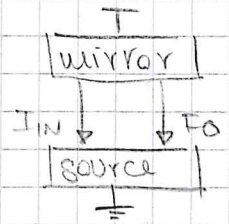




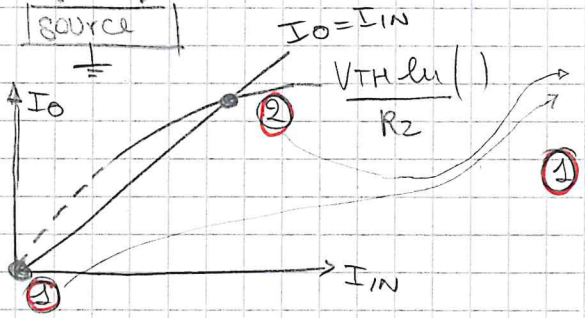
$$I_O = \frac{V_{TH} \ln\left(\frac{I_{IN}}{I_S}\right)}{R_2}$$ → This equation is valid for some positive I_{IN} quantity.

Our goal is to have $I_{IN} = I_{OUT}$ w/o dependancy on V_{CC}

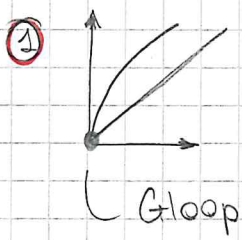
Ideal Mirror

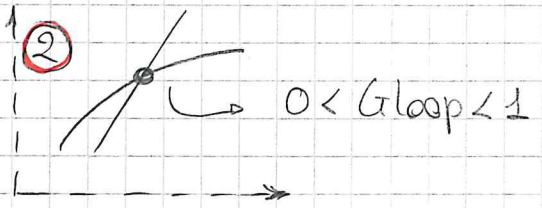


- Source imposes a ln characteristic
- Mirror imposes $I_{IN} = I_{OUT}$



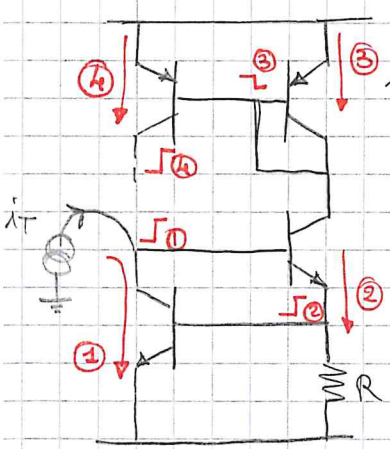
We have two working points:



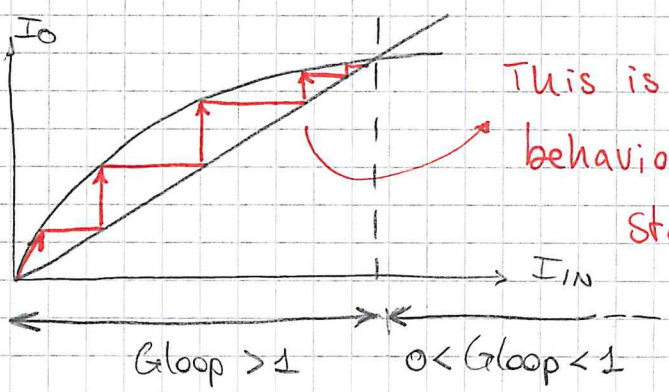


First point is critical. At turn-on, the circuit will stick to this exact $I_O = I_{IN} = 0$ because Gloop > 1

We need a <u>startup circuit</u> that excites the current mirror so that we reach point (2)



→ Always check that Gloop > 0 for this reference

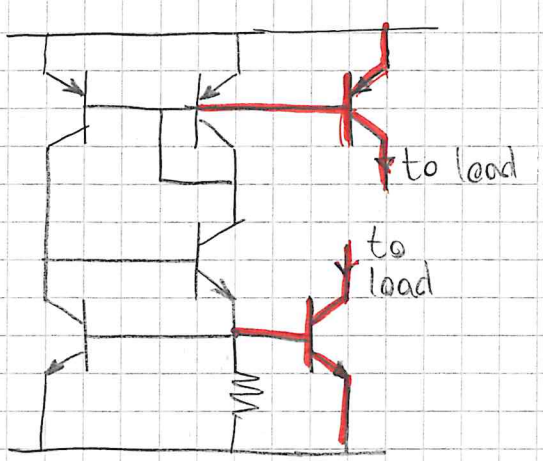


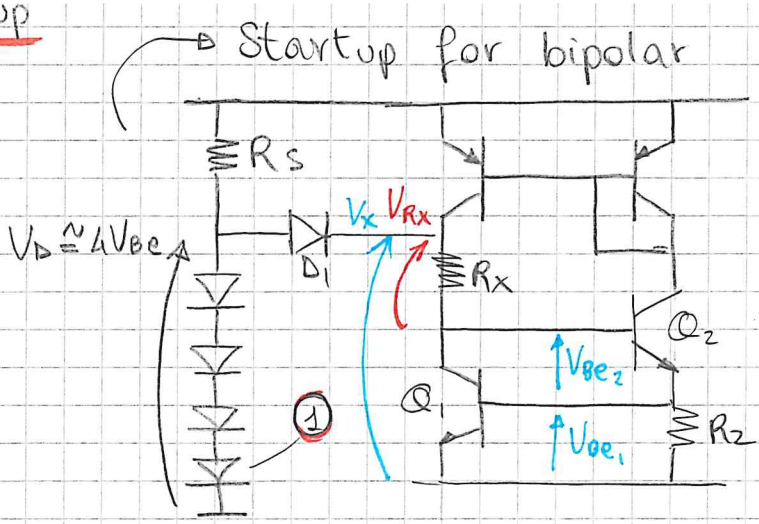
This is the startup behaviour using the startup circuit

Startup circuit is mandatory (not shown here).

Note: this circuit is still sensitive to <u>process/temperature</u>

Deriving sources + startup



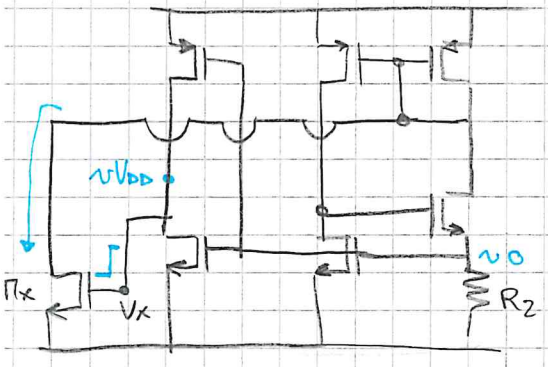


① These diodes are typically implemented with transistors

At startup, when V_x is large enough to shut D_1 off it means that we moved away from $I_{IN} = I_{OUT} = \cancel{0}$

$V_x = 2V_{BE} + I_{IN}R_x$ → R_x needs to be large enough so that D_1 shuts off correctly

CMOS bootstrap startup circuit



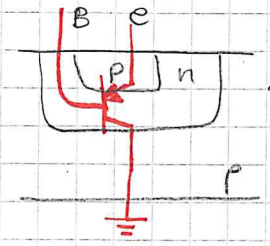
We use a CMOS inverter:

- At startup $I_O = 0$ then $V_{R_2} \sim 0$
- Inverter changes voltage → $V_x \cong V_{DD}$
- M_x sucks current so we go to the right working point.

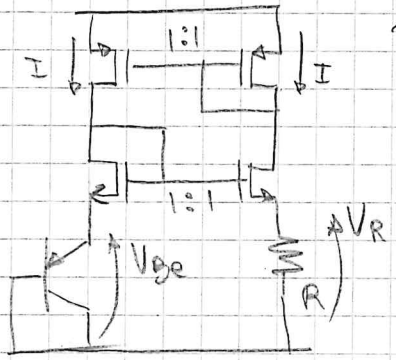
nMOS needs to be sized so that when V_{R_2} = constant, the inverter shuts off → $nMOS|_{INV}$ is larger than $pMOS|_{INV}$

(See Digital design notes)

3+) CMOS parasitic V_{BE} reference



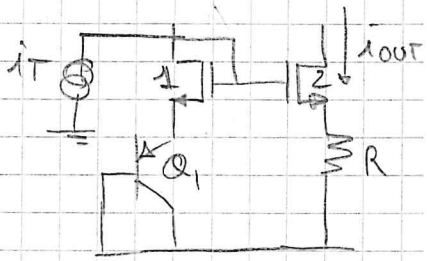
→ This device can be made using CMOS technology, but: it's slow, β is small (large W_B), collector is connected to the bulk. However, we just need a diode in order to build a V_{BE} reference!



↳ missing startup circuit but needed!

If $I_{IN} = I_{OUT}$, $V_R = V_{BE_1}$ $\quad I = V_{BE_1}/R$

Is $G_{loop} < 1$?



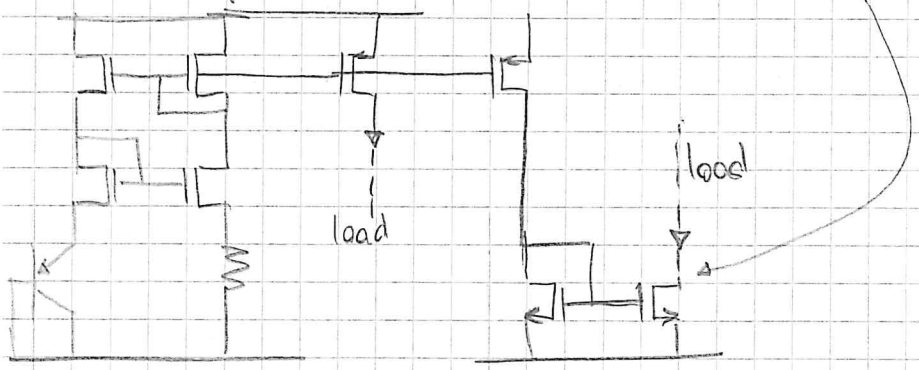
$$i_{OUT} = \frac{1/g_{m_1} + 1/g_{mQ_1}}{R + 1/g_{m_2}} \cdot i_T \rightarrow < 1\ ?$$

$$\frac{1}{g_{m_1}} + \frac{1}{g_{mQ_1}} < R + \frac{1}{g_{m_2}}$$

↳ $G_{loop} < 1$ if $g_{mQ_1} R > 1 \rightarrow \underline{V_{BEQ_1} > V_{TH}}$

We verified that $G_{loop} < 1$

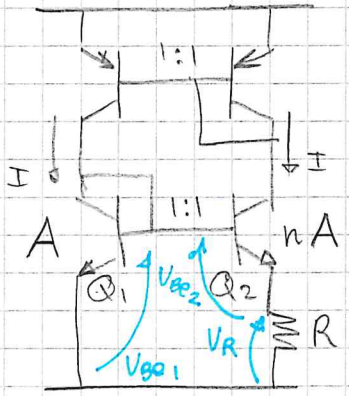
Note: if we wanted a low side current ref:



38) PTAT V_{TH} current reference

We want to generate a current reference that is proportional to temperature → Proportional to absolute temp

We will use PTAT references to either build temperature sensors or to build BGR (see later).



V_{TH} is absolute-dependant on temperature.

To measure it we can pick the difference between two V_{BE}:

Q_2 has larger area (nA) wrt Q_1 (n) so

$V_{BE1} > V_{BE2}$ → we will see a drop on R

$$V_R = V_{BE1} - V_{BE2} = V_{TH}\left[\ln\left(\frac{I}{I_{S1}}\right) - \ln\left(\frac{I}{I_{S2}}\right)\right] = V_{TH}\ln\left(\frac{I_{S2}}{I_{S1}}\right) =$$

$$V_{BE1} - V_{BE2} = V_{TH}\ln\left[\frac{nI_S}{I_S}\right] = V_{TH}\ln[n]$$

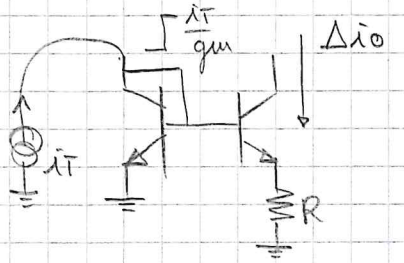
$$I = \frac{V_{TH}\ln[n]}{R}$$

Note: if T↗ also R can be proportional to temperature → R↗ but V_{TH}↗ ⇒ I ~ const

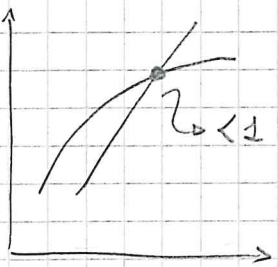
We need to know the kind of dependance of R with temperature

NOTE: Startup is missing!

Is $G_{loop} < 1$?

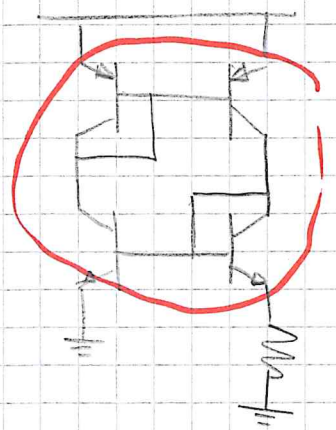


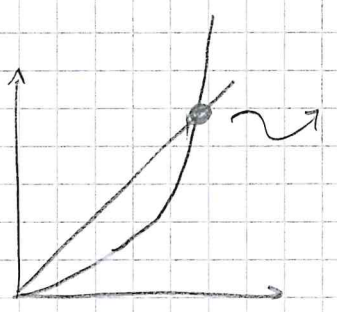
$$\frac{\Delta i_o}{\Delta T} \cong \frac{1/g_m}{\frac{1}{g_m} + R}$$ ⇝ clearly < 1



Curious note: switch mirrors connections

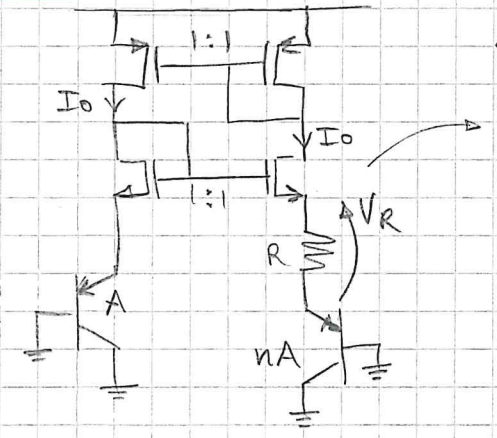
NO





$G_{loop} > 1$ VERY BAD!

39) CMOS implementation of V_{TH} PTAT ref



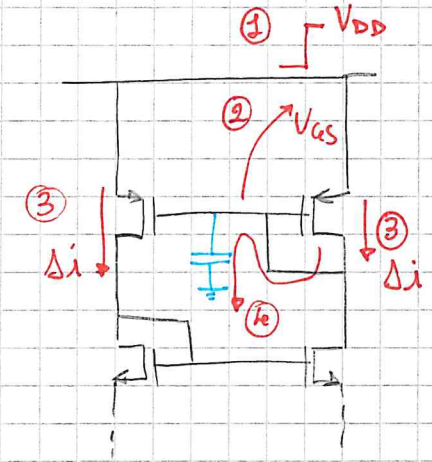
Startup circuit is missing

This is not a mirror since there is only one value for which ratio is 1:1, which is the working point itself

$V_R = V_{BE,1} - V_{BE,2} = V_{TH} \ln[n]$

$I_{IN} = I_O = \frac{V_{TH} \ln[n]}{R}$ ⇝ PTAT!

Note on V_{DD} disturbs:



① V_{DD} steps, voltage on C cannot change immediately

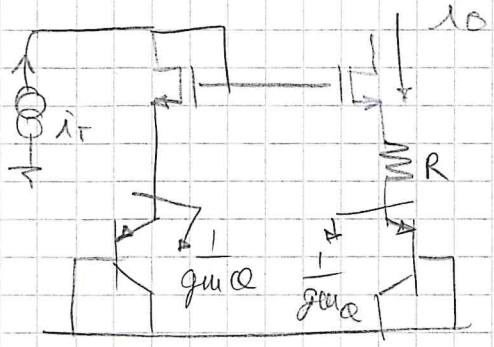
② V_{GS} momentarily increases

③ because of ②, a Δi current flows into the source, but since there is only one working condition, the source rejects the current change

thanks to the Gloop correction

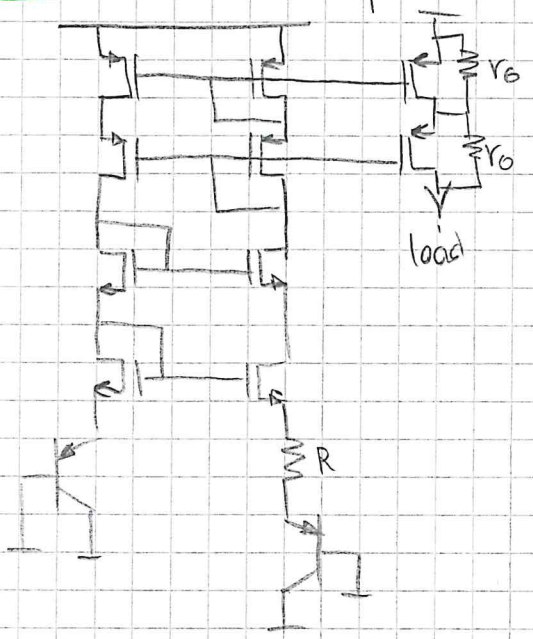
④ the rejected current flows into C so that V_{GS} returns to the correct, final value that allows $I_{IN} = I_O$

Is Gloop < 1?

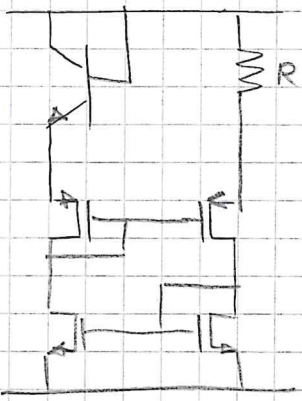


$i_O = i_T \dfrac{\frac{1}{g_{mn}} + \frac{1}{g_{mp}}}{\frac{1}{g_{mn}} + \frac{1}{g_{mp}} + R}$ < 1 for sure!

4U) Cascoded ref. and other miscellaneous references:

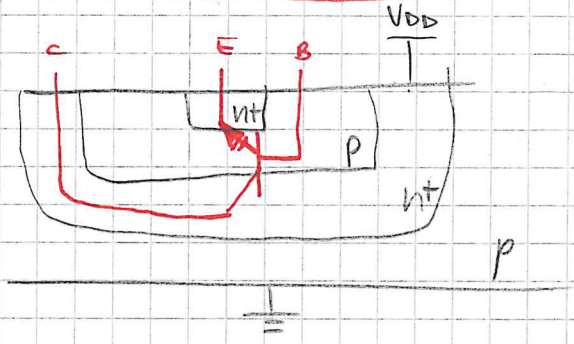


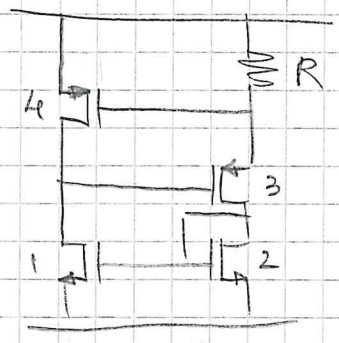
If $V_{DD} > 1$, we can allow r_o increase through cascodes. We typically cascode the output transistor as well!



High-side referred V_{BE-REF}:

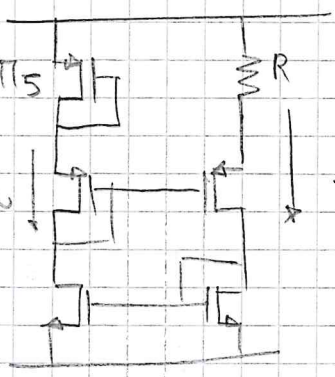
The npn is:





Other high-side V_{GS-REF}

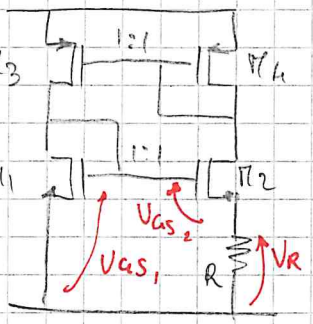
$$I_1 = I_o = \frac{V_{GS4}}{R} = \frac{|V_{TP}| + V_{OV4}}{R}$$



Other V_{GS-REF}

$$I_o = \frac{V_{GS5}}{R}$$

4.1) Constant g_m current reference



We would like a CMOS current reference that works with low V_{DD} that is "insensitive" to temperature and voltage supply.

If $I_{IN} = I_{OUT}$, then $V_{GS1} = V_{GS2} + IR$

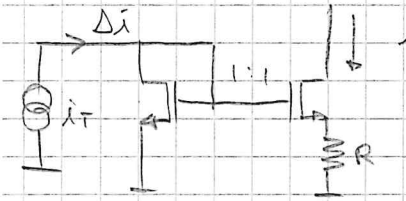
$$\sqrt{\frac{2I}{\mu C_{ox}\left(\frac{W}{L}\right)_n}} + V_T = \sqrt{\frac{2I}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n K}} + V_T + IR$$ where K is a multiplying factor.

$$\sqrt{\frac{2I}{\mu_n C_{ox}\left(\frac{W}{L}\right)}}\left(1 - \frac{1}{\sqrt{K}}\right) = IR \qquad \frac{2I}{\mu_n C_{ox}\left(\frac{W}{L}\right)}\left(1 - \frac{1}{\sqrt{K}}\right)^2 = I^2 R^2$$

$$I_O = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)} \frac{1}{R^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2 \quad (3)$$

↳ Does not depend on V_{DD} and temperature dependance may come from μ, R values

Loop gain check:



$$i_O = \frac{\Delta i}{g_{m1}} \cdot \frac{1}{R + 1/g_{m2}}$$ where $g_{m2} = \sqrt{K}\, g_{m1}$

↳ Is it < 1?

$$\frac{1}{g_{m1}R + \frac{1}{\sqrt{K}}} < 1 \qquad R > \frac{1}{g_{m1}}\left(1 - \frac{1}{\sqrt{K}}\right) \longrightarrow \text{let us reason:}$$

- ① R is > 0
- ② $\frac{1}{g_{m1}}\left(1 - \frac{1}{\sqrt{K}}\right) > 0$ (of course)

→ Since ①, ② are true, then $R^2 > \frac{1}{g_{m1}^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2$ is true

Does this statement make sense? See:

$$R^2 > \frac{1}{2\mu C_{ox}\left(\frac{W}{L}\right)_n \frac{I}{}}\left(1 - \frac{1}{\sqrt{K}}\right)^2$$ → We basically found the same equation of ③, thus this last statement must be true as well, therefore $G_{loop} < 1$

The origin of constant g_m name

$$I = \frac{2}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n} \cdot \frac{1}{R^2}\left(1-\frac{1}{\sqrt{K}}\right)^2 \quad \text{Compute } g_{m_1}$$

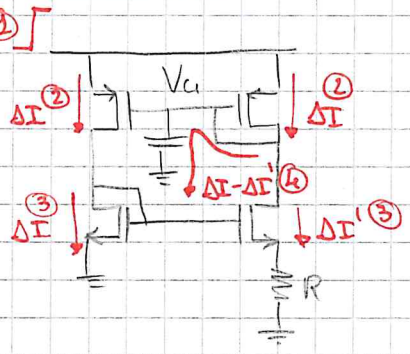
$$g_{m_1} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_n I} = \sqrt{2}\sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)_n} \cdot \frac{\sqrt{2}}{\sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)_n}} \cdot \frac{1}{R}\left(1-\frac{1}{\sqrt{K}}\right)$$

$$g_{m_1} = \frac{2}{R}\left(1-\frac{1}{\sqrt{K}}\right) \quad \text{common } K \text{ value is } K=4$$

Since K needs to be integer (because it multiplies transistors areas), we get $g_{m_1}\big|_{K=4} = \frac{1}{R}$ → R sets the g_m value → constant

$g_{m_2} = \sqrt{K}\, g_{m_1} = \frac{2}{R}$

V_{DD} step



① V_{DD} rises (step)

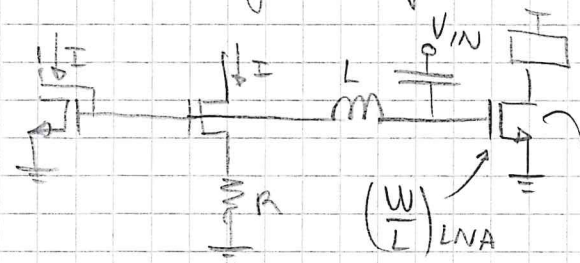
② V_{GS_3}, V_{GS_4} increases and a ΔI is generated

③ Since the mirror is unbalanced, we see a ΔI and $\Delta I'$ currents

④ $\Delta I - \Delta I'$ flows into C, V_a rises until C is fully charged and transient stops

RF circuits biasing:

Constant g_m ref are usually used to bias RF stages:

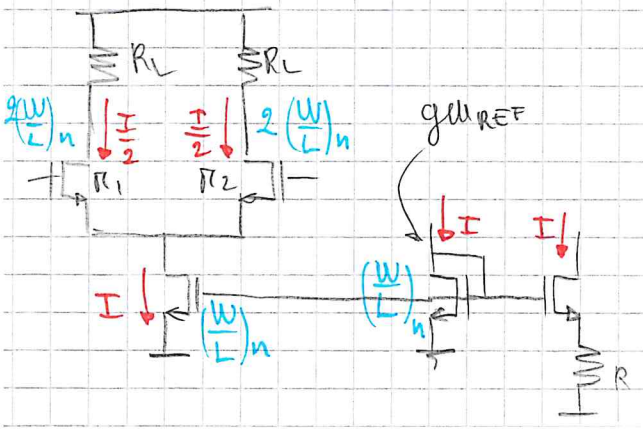


g_m is set by R value

$g_m\big|_{LNA} \propto \frac{1}{R}$ and its $\left(\frac{W}{L}\right)_{LNA}$

Diff pair biasing: → $A_{DD} = g_{m_{1,2}} R_L$, but $I_{1,2} = \frac{I}{2}\Big|_{REF}$

and $\left(\frac{W}{L}\right)_{1,2} = 2\left(\frac{W}{L}\right)_{REF}$



Therefore $g_{m_{1,2}} = g_{m_{REF}} = \frac{1}{R}$

and $A_{DD} = \frac{R_L}{R}$

Gain is precisely set, accuracy depends on resistors relative mismatch only! QL

42) BGR : band gap reference

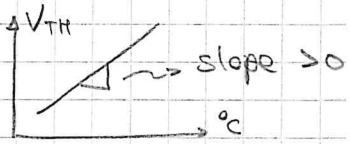
Considered "the cutest circuit ever designed" it should be to first order insensitive to temperature

$\frac{\partial V_{REF}}{\partial T} = 0$ In the end, BGR turns out to be insensitive to both P, V, T variables (process, voltage, temperature).

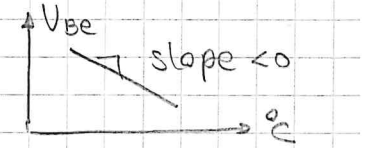
Since it depends on bandgap → insensitive to process.

So far, we saw:

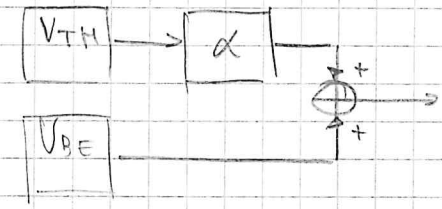
- V_{TH} ref (PTAT) $\frac{\partial V_{TH}}{\partial T} = \frac{V_{TH}}{T} = \frac{k}{q} \simeq 0{,}085\ mV/°C$



- V_{BE} ref (CTAT) (→ complementary) $\frac{\partial V_{BE}}{\partial T} \simeq -2\ mV/°C$



If we cancel the slopes by summing them → Constant voltage!

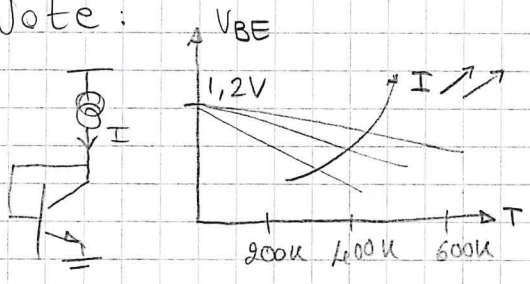


If we correctly set a gain α on V_{TH}:

$V_{REF} = \alpha V_{TH} + V_{BE}$ $\quad \frac{\partial V_{REF}}{\partial T} = \alpha \left(\frac{V_{TH}}{T}\right) + V_{BE} = 0$

e.g.: $\frac{\partial V_{BE}}{\partial T} = -2\ mV/°C$ then $\alpha = \frac{2}{0{,}085} \simeq 24$

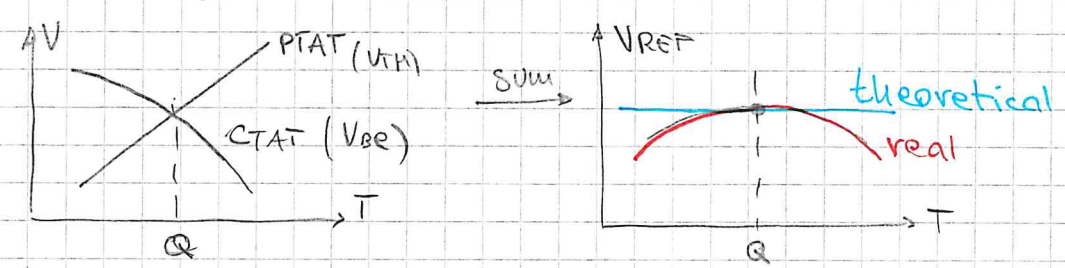
Note:



↳ V_{BE} depends on I_C, all points converge to a single voltage ~1,2V

When we change I → we must adjust α

Issue: V_{BE} is a little bit convex:



So, when V_{TH} and V_{BE} are summed, we still have some dependance on T change.

V_{BE} dependance on T

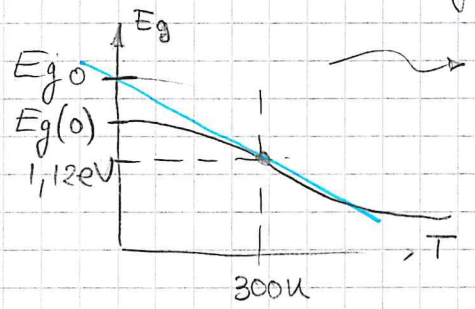
$V_{BE} = V_{TH} \ln\left(\frac{I_C}{I_S}\right)$ ⇝ We can say $V_{BE} \propto V_{TH}$ ④ → Wrong!

We need to take into account I_S dependancy on temperature:

① $I_C = I_S \exp\left(\frac{V_{BE}}{V_{TH}}\right) \Rightarrow A_q D_n \frac{n_i^2}{N_A W_B}$; $n_i^2 \propto T^3 e^{-E_g/kT}$; $D_n = \mu_n \frac{kT}{q}$ → $\mu_n \propto T^m = T^{\frac{-3}{2}}$

② $I_S = b\,T^{m+4} \exp\left(-\frac{E_g}{kT}\right)$ → depends expouentially on temperature!

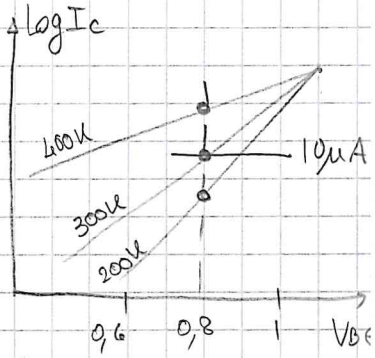
It's worth noting that E_g depends on T as well:



$E_g(0)$ = real energy gap @ 0K (not measurable)

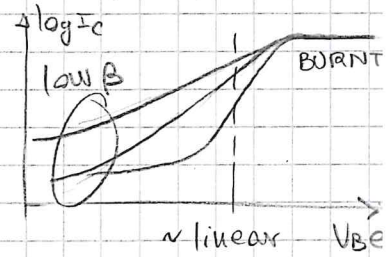
E_{go} = theoretical energy gap interpolated from the 300K measurement (found in literature) $E_{go} = 1,205\,eV$

Plug ② into ① and $I_C \cong b T^{m+4} \exp\left(\frac{V_{BE} - E_g/q}{kT/q}\right)$



Actually, the slope will be linear only at center:

- Large V_{BE} → burnt device
- too small V_{BE} → low bias and → β issues



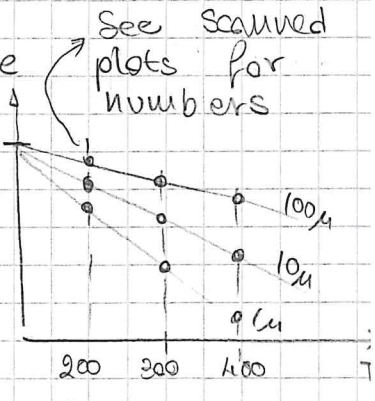
What's the increase for a ×10 I_C change?

$$\begin{cases} \ln I_C - \ln I_S = \frac{V_{BE}}{V_{TH}} \\ \ln 10 I_C - \ln I_S = \frac{V_{BE} + \Delta V_{BE}}{V_{TH}} \end{cases} \rightarrow \Delta V_{BE} = V_{TH} \ln 10 \cong 60\,mV$$ ③

So, slopes change with temperature:

- 300K → 60mV/dec ③
- 400K → 80mV/dec
- 200K → 40mV/dec

→ V_{BE} does not depend on V_{TH} only ④



Let us derive $V_{BE} \propto T$ equation. Assume $C = b T^{m+4}$, then:

$$I_C = C \exp\left(\frac{-E_g/q + V_{BE}}{kT/q}\right) \rightarrow V_{BE} = \frac{kT}{q} \ln\left[\frac{I_C}{C}\right] + \frac{E_g}{q} = -\frac{kT}{q} \ln\left[\frac{C}{I_C}\right] + \frac{E_g}{q}$$

($\ln[I_C/C] < 0$)

@ 0K → $V_{BE} = 1,2\,V$ correct. C is considered constant with T

BGR full computation

$V_{BE} = -\frac{KT}{q} \ln\left[\frac{C}{I_C}\right] + \frac{E_g}{q}$ ↝ This is not enough since we considered C to be constant with temperature. However $C = b\,T^{m+4}$ → let us do the full discussion

↳ convex dependance!

Compute the V_{BE} complete temperature dependance:

$V_{BE} = V_{TH} \ln\left(\frac{I_C}{I_S}\right) \rightarrow \frac{\partial V_{BE}}{\partial T} = \frac{V_{TH}}{T} \ln\left(\frac{I_C}{I_S}\right) + V_{TH} \cdot \frac{1}{\cancel{I_C}} \left(\frac{\partial I_S}{\partial T}\right) \frac{\cancel{I_C}}{I_S^2}$

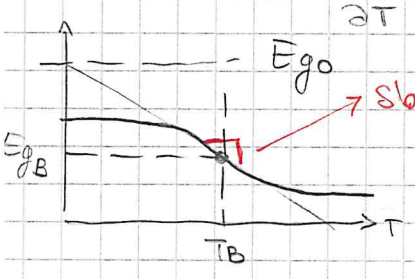
(V_{TH}: ↳ $f(T)$, I_S: ↳ $f(T)$)

For a specific bias point B given by fixed T, I then:

$$\left.\frac{\partial V_{BE}}{\partial T}\right|_B = \left(\frac{V_{TH}}{T}\right)_B \ln\left[\frac{I_C}{I_S}\right]_B - \underbrace{\left(\frac{V_{TH}}{I_S}\frac{\partial I_S}{\partial T}\right)_B}_{②}$$

Since $I_S = b\,T^{m+4} \exp\left(-\frac{E_g}{KT}\right) \rightarrow \frac{\partial I_S}{\partial T} = b(m+4)T^{m+3} e^{\left(\frac{-E_g}{KT}\right)} + bT^{m+4}\left(\frac{E_g}{KT^2} - \frac{1}{KT}\frac{\partial E_g}{\partial T}\right)$ ①

We now need $\frac{\partial E_g}{\partial T}$, but since we selected T_B, I_B (working point B):



$\frac{\partial E_g}{\partial T} = -\frac{E_{g0} - E_{gB}}{T_B}$ then we can solve

① $\frac{E_g}{KT^2}\left(1 - \frac{T}{E_g}\frac{\partial E_g}{\partial T}\right) = \frac{E_{gB}}{KT_B^2}\left[1 + \frac{T_B}{E_{gB}} \cdot \frac{E_{g0} - E_{gB}}{T_B}\right]$

Now we can complete ②:

$$\left(\frac{V_{TH}}{I_S}\frac{\partial I_S}{\partial T}\right)_B = \left(\frac{V_{TH}}{I_S}\right)_B \left(\frac{\partial I_S}{\partial T}\right)_B = V_{TH_B}\left[\frac{\cancel{b}(m+4)\cancel{T_B^{3+m}}\,e^{-\frac{E_{g0}}{KT_B}}}{\cancel{b}\,T^{m+4}\,e^{-\frac{E_{g0}}{KT_B}}} - \frac{\cancel{b\,T_B^{m+4}}\,e^{-\frac{E_{g0}}{KT_B}} \cdot \frac{E_{g0}}{KT_B^2}}{\cancel{b\,T_B^{m+4}}\,e^{-\frac{E_{g0}}{KT_B}}}\right]$$

② $= \frac{V_{TH_B}}{T_B}(m+4) - V_{TH_B}\frac{E_{g0}}{KT_B^2}$ So we finally say

$$\left(\frac{\partial V_{BE}}{\partial T}\right)_B = \left(\frac{V_{TH}}{T}\right)_B \ln\left[\frac{I_C}{I_S}\right]_B - \left(\frac{V_{TH}}{I_S}\frac{\partial I_S}{\partial T}\right)_B = \frac{V_{BE_B} - (4+m)V_{TH_B} - E_{g0}/q}{T_B}$$

e.g: $V_{BE_B} = 0{,}7V$ $\quad m = -\frac{3}{2}$ $\quad T = 300K$ $\quad \frac{E_{g0}}{q} = 1{,}205V$

↳ Set current I_C on point B, same thing for temperature

We get $\left(\frac{\partial V_{BE}}{\partial T}\right)_{B \rightarrow T=300K,\ V_{BE}=0{,}7V} \cong -1{,}89\ mV/K$

Given this last value, now we need to untill α

$$V_{REF} = V_{Be} + V_{TH}\,\alpha \longrightarrow \left(\frac{\partial V_{REF}}{\partial T}\right)_B = \left(\frac{\partial V_{Be}}{\partial T}\right)_B + \alpha\left(\frac{V_{TH}}{T}\right)_B = 0$$

So we enforce

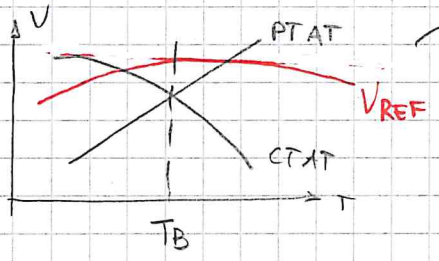
$$\left(\frac{\partial V_{Be}}{\partial T}\right)_B = \alpha\left(\frac{V_{TH}}{T_B}\right)_B \longrightarrow -\alpha\frac{V_{TH_B}}{T_B} = \frac{V_{Be_B} - (A+m)\,V_{TH_B} - E_{g_0}/q}{T_B}$$

↳ optimum alfa

$$\alpha\Big|_{opt} = -\frac{V_{Be_B}}{V_{TH_B}} + (A+m) + \frac{E_{g0}}{V_{TH_B}\cdot q}$$

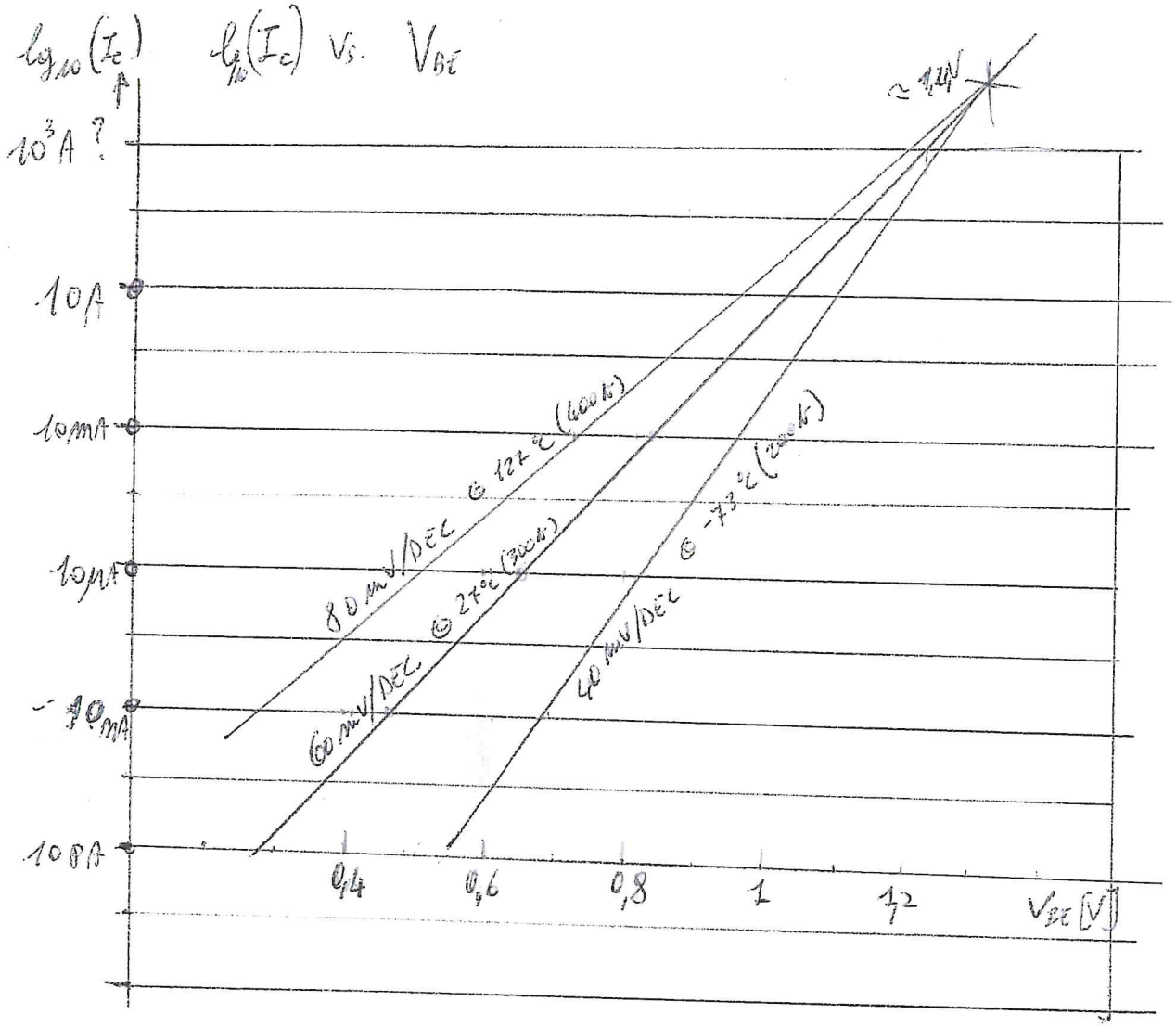
$$V_{REF}\Big|_B = \frac{E_{g0}}{q} + (A+m)\,V_{TH_B}$$ ↳ Source of the name "Bandgap reference"

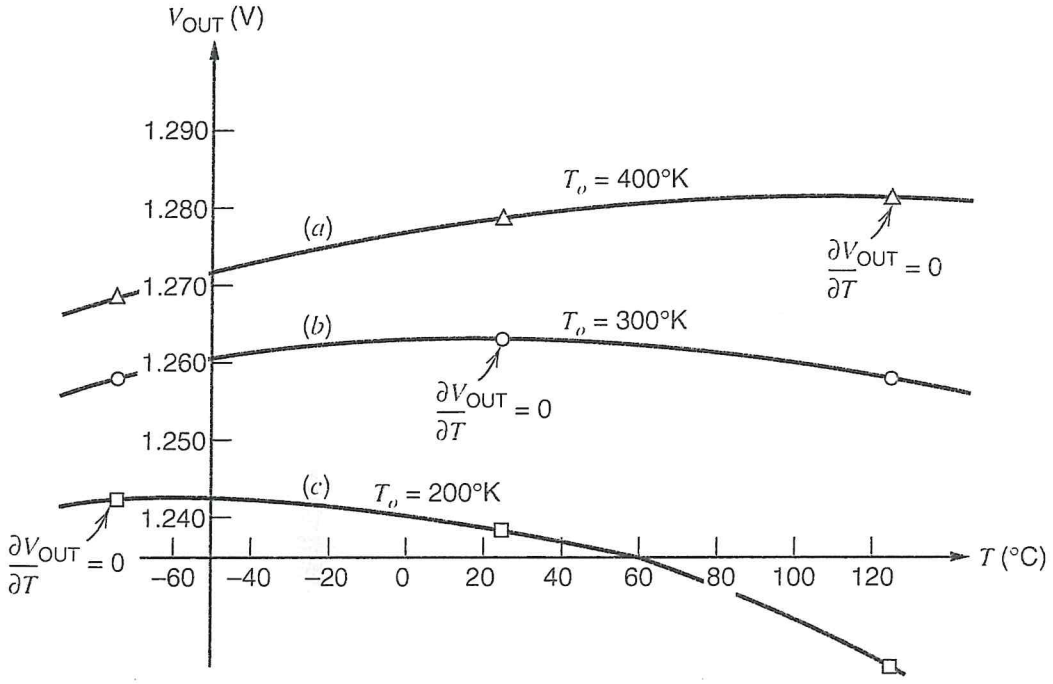
Depending on m value, we get $V_{REF}\Big|_B \simeq 1{,}26\ldots\ V$



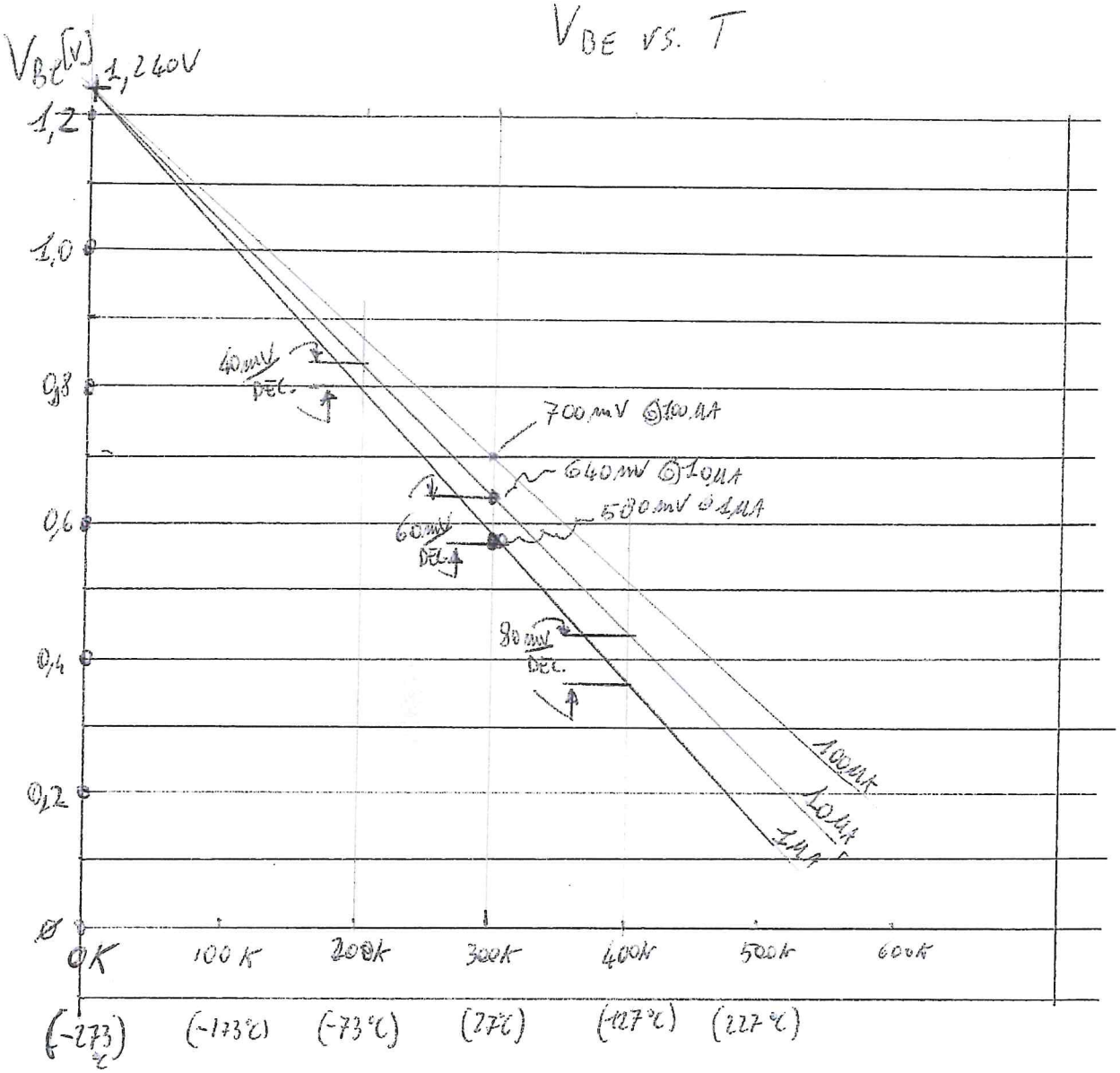
↳ Curvature is small. However, there are some circuits called "curvature correction" that take care of the deviation.

Therefore, in order to correctly design the BGR we need a working point.

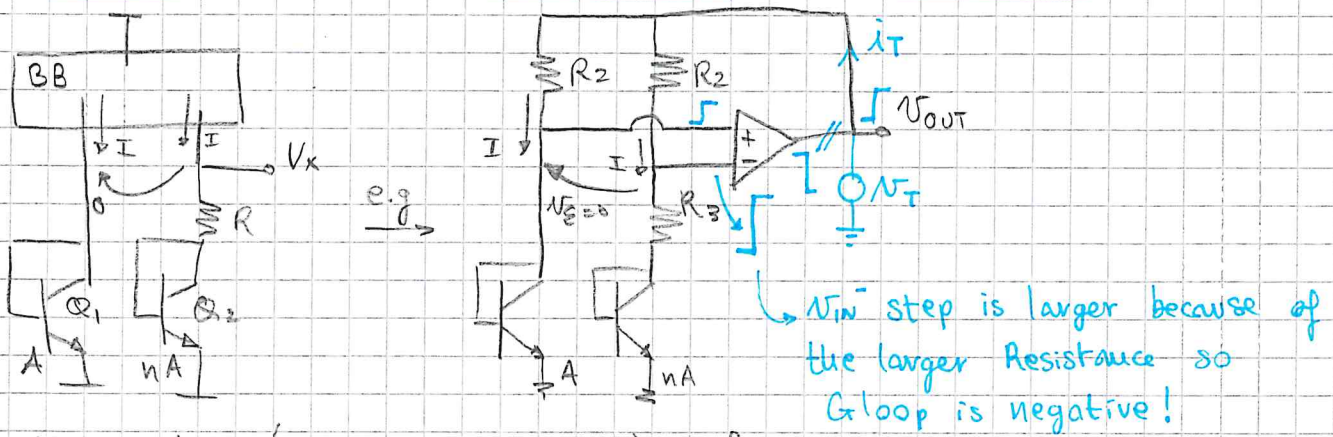

$\log_{10}(I_C)$ vs. V_{BE}
10^3A ?
1 A
10 mA
1 mA
100 µA
10 µA
≃ 1,4V
80 mV/DEC @ 127°C (400 K)
60 mV/DEC @ 27°C (300 K)
40 mV/DEC @ -73°C (200 K)
0,4
0,6
0,8
1
1,2
V_{BE} [V]



(*source: Analysis and Design of Analog Integrated Circuits – P. Gray, P. Hurst, S. Lewis, R. Meyer, 5th Ed., John Wiley & Sons, 2009*)


V_{BE} vs. T
V_{BE} [V]
1,240V
1,2
1,0
0,8
0,6
0,4
0,2
0
40mV/DEC.
700mV @100µA
640mV @10µA
580mV @1µA
60mV/DEC.
80mV/DEC.
100µA
10µA
1µA
0K
100K
200K
300K
400K
500K
600K
(-273°C)
(-173°C)
(-73°C)
(27°C)
(127°C)
(227°C)

43) BGR circuit implementations : Kuijk circuit



The Black box (opamp + R_2 circuit) enforces the same current on the two branches so $V_R = V_{BE1} - V_{BE2} = IR = V_{TH} \ln[n]$ and

$V_X = V_{BE} + V_{TH} \ln[n]$ ⇝ since $\alpha \sim 24$, $n = e^{24} = 2{,}7 \cdot 10^{10}$ ⟶ Not implementable

Consider now the opamp circuit (Ideal opamp):

If feedback is ∞ and <0, then $V_\xi = 0$ ⟶ $I_{R_2} = I_{R_2} = I$

We see that $V_O = V_{REF}$ $V_{R_3} = V_{TH} \ln[n]$ ⇝ sets the current

$$I = \frac{V_{R_3}}{R_3} = \frac{V_{TH} \ln[n]}{R_3} \qquad V_{REF} = V_{BE_2} + I(R_2 + R_3) = V_{BE_2} + V_{TH} \ln[n] \left(1 + \frac{R_2}{R_3}\right)$$

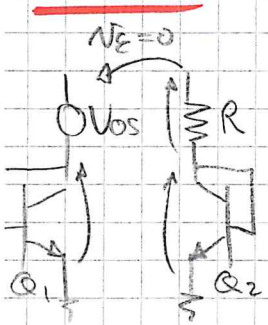
Now we can design a true BGR → $\alpha = \ln[n] \left(1 + \frac{R_2}{R_3}\right)$

If α is properly selected $V_{REF} = \frac{E_{g0}}{q} + (4+m) V_{TH_B}$

If we wanted to relax $\ln[n]$ requirement: R_3 sets the current value so it can't be changed, while R_2 can be increased

However, check that Gloop remains negative

Issues: suppose that the opamp is affected by V_{OS}:



⇝ $V_{BE_1} + V_{OS} \cong V_{BE_2} + R_3 I_{C_2}$ $I_{C_2} = \frac{V_{BE_1} - V_{BE_2} + V_{OS}}{2}$

$$I_{C_2} = \frac{V_{TH} \ln[n] + V_{OS}}{R_3} \quad \text{and it follows that}$$

$$V_{REF} = V_{BE} + I_{C_2}[R_2 + R_3] = V_{BE_2} + (V_{TH} \ln[n] + V_{OS}) \left(1 + \frac{R_2}{R_3}\right)$$

V_{OS} is detrimental to the reference voltage (expected).

We need a large $\ln[n]$ so V_{REF} is less sensitive to V_{OS}

I_C dependance on T for the Kuijk circuit

$I_C = \frac{V_{TH} \ln[n]}{R_3}$ ① when computing the $\frac{\partial V_{BE}}{\partial T}$, we stated that only V_{TH} and I_S were $f(T)$ while I_C did not depend on T. This is not true! Look at ①, there is V_{TH}!

Rewrite the previous $\partial V_{BE}/\partial T$:

$$\frac{\partial V_{BE}}{\partial T} = \underbrace{\frac{V_{TH}}{T} \ln\left[\frac{I_C}{I_S}\right] - V_{TH}\left(\frac{\partial I_S}{\partial T}\right)}_{\text{previous expression}} + \underbrace{\frac{V_{TH}}{\frac{I_C}{I_S}} \cdot \frac{1}{I_S} \frac{\partial I_C}{\partial T}}_{\text{new addition}} \quad ②$$

So, by considering ① for the Kuijk implementation:

$$\frac{\partial I_C}{\partial T} = \frac{I_C}{T} \quad \text{so} \quad ② = \frac{V_{TH}}{I_C} \cdot \frac{I_C}{T} = \frac{V_{TH}}{T}$$

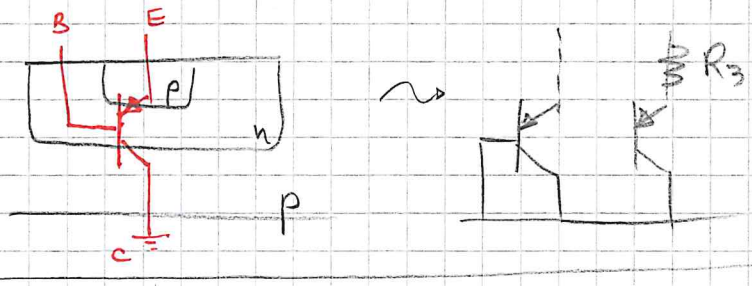
Therefore we add ② to the previous result

$$\frac{\partial V_{BE}}{\partial T} = \underbrace{\frac{V_{BE}}{T} - (4+m)\frac{V_{TH}}{T} - \frac{V_{TH}}{T}\frac{E_{g0}}{KT}}_{\text{previous}} + \underbrace{\frac{V_{TH}}{T}}_{\text{new}} = \frac{V_{BE} - (3+m)V_{TH} - \frac{E_{g0}}{q}}{T}$$

And, if the BGR is well designed $V_{REF}\big|_B = \frac{E_{g0}}{q} + (3+m)V_{TH_B}$

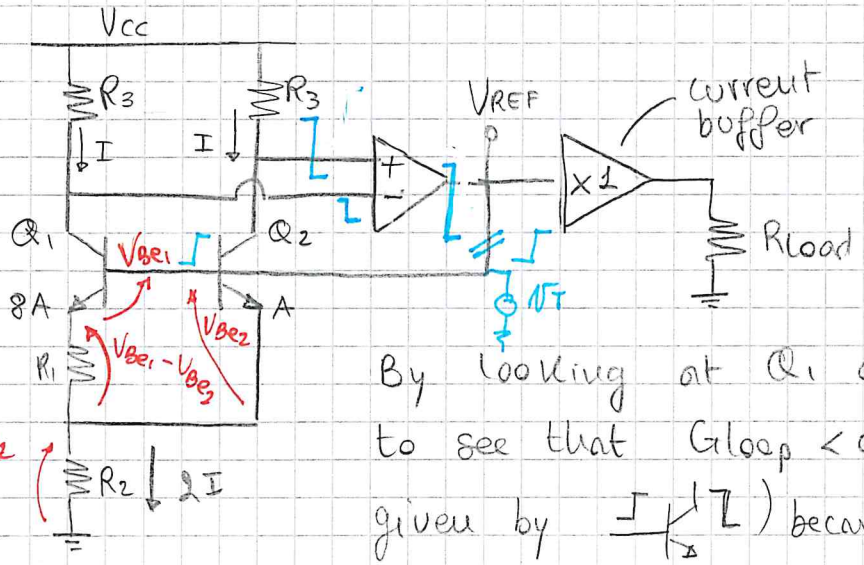
Therefore the previous $(4+m)$ now becomes $(3+m)$

CMOS bipolar BGR: we can implement the Kuijk circuit using the shitty bipolar transistors:



Since $V_{REF} = 1,2$ and $V_{DD} \sim 1V$, we will have higher breakdown voltage transistors used in the BGR section in the IC. However, most of the times technology already allows for a $\sim 1,8$ Breakdown voltage.

44) Brokaw BGR



$R_1 = 1\,K\Omega$

$R_2 = 4,619\,K\Omega$

$R_3 = 40K\,\Omega$

$T = 300\,K$

By looking at Q_1 degeneration it's trivial to see that $G_{loop} < 0$ (sign inversion is given by $\frac{I}{I_1}$) because less i flows through Q_1 wrt Q_2.

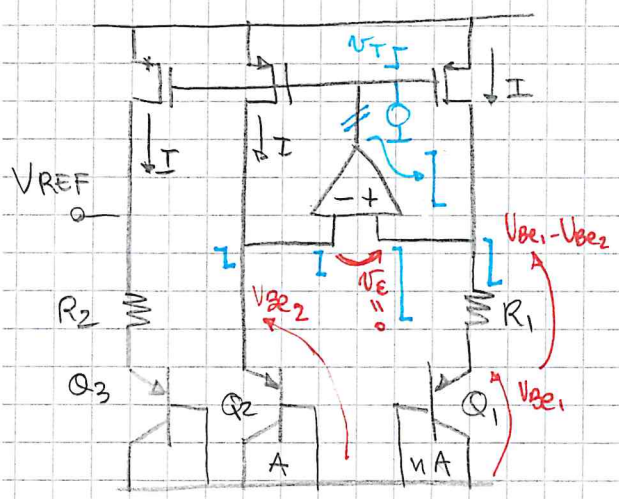
$$V_{BE_1} - V_{BE_2} = V_{TH}\, ln[8] \longrightarrow I_1 = I = \left.\frac{V_{TH} ln\, 8}{1K\Omega}\right|_{T=300K} = 53,6\,\mu A$$

$$V_{R_2} = 2I \cdot R_2 = \frac{2\, V_{TH}\, ln\, 8}{1K\Omega}\, 4,619\,K\Omega = 19,2\, V_{TH}$$

$$V_{REF} = V_{BE_2} + 19,2\, V_{TH} \longrightarrow = \frac{E_{g0}}{q} + (4+m)\, V_{TH_B}$$

$$V_{REF} = V_{BE_2} + V_{TH}\, ln[n] \cdot \frac{R_2}{R_1}$$

45) CMOS BGR examples



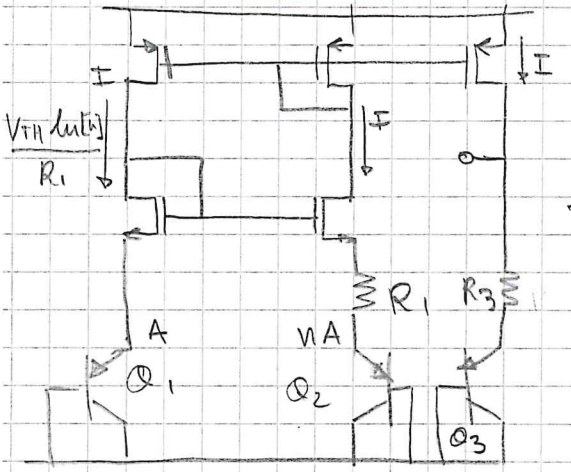
$I = V_{R_1} / R_1$ Gloop < 0 | R_1 branch has larger resistance so voltage step on V_{IN}^+ is higher)

$V_{R_1} = I \cdot R_1 = V_{TH} \ln[n]$

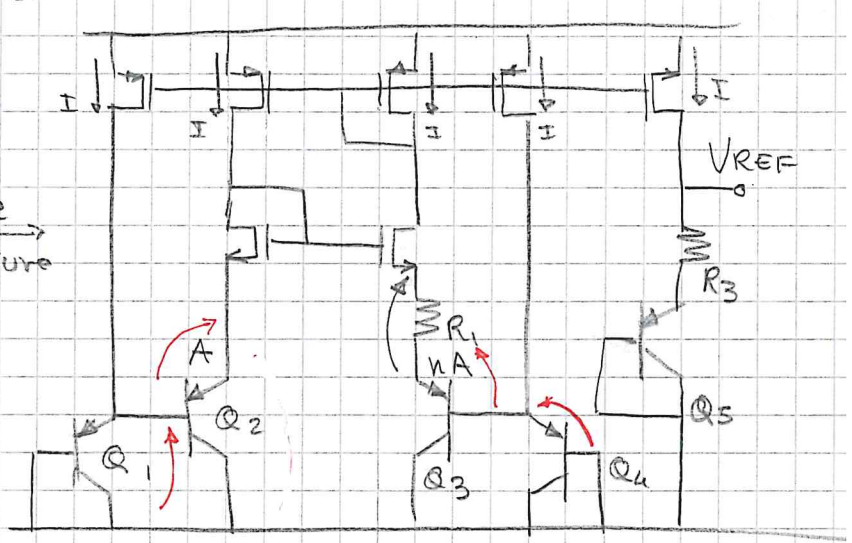
$V_{REF} = V_{BE_2} + \left(\frac{R_2}{R_1}\right) V_{TH} \ln[n]$

Remember that we absolute need an output buffer for V_{REF}

Another example: positive feedback BGR



double structure →



$V_{BE_3} + \frac{R_3}{R_1} \ln[n] V_{TH} = V_{REF}$

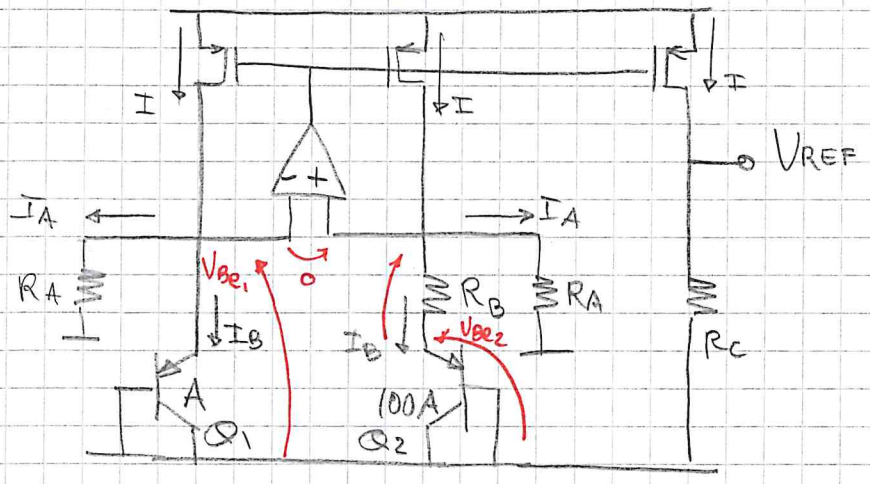
For the double structure:

$$I_{R_1} = \frac{(V_{BE_1} + V_{BE_2}) - (V_{BE_3} + V_{BE_4})}{R_1} = \frac{2 V_{TH} \ln[n]}{R_1} = I$$

$$V_{REF} = V_{BE_5} + 2 V_{TH} \ln[n] \frac{R_3}{R_1} \xrightarrow{OS} V_{REF} = V_{BE_5} + [2 V_{TH} \ln[n] + V_{OS}] \frac{R_3}{R_1}$$

Since we get a x2 factor on $V_{TH} \ln$, V_{OS} will have less influence. However, we're not considering low β, r_o, mismatches, etc... so it's not a great design

46) CMOS low voltage BGR



$I = I_A + I_B$ left and right I_A, I_B can be considered equal to first order because of the ideal opamp ($v_\varepsilon \to 0$)

$$I_B = \frac{V_{TH}\, ln\, 100}{R_B} \qquad I_A = \frac{V_{BE1}}{R_A} \qquad V_{REF} = R_C \left[\frac{V_{TH}\, ln\, 100}{R_B} + \frac{V_{BE1}}{R_A} \right]$$

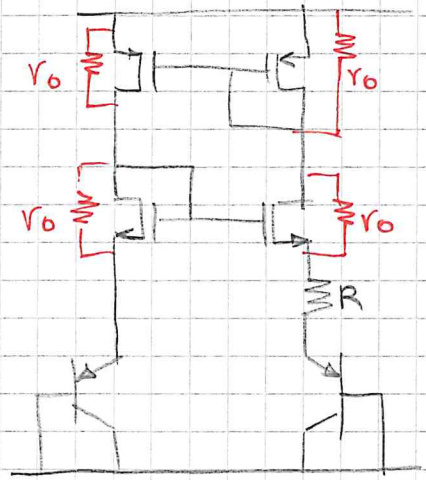
$$V_{REF} = \frac{R_C}{R_A} \left[V_{BE1} + V_{TH}\, ln(100)\, \frac{R_A}{R_B} \right]$$

e.g.: $R_A = 2{,}063\ M\Omega$ $R_B = 39{,}3\ M\Omega$ $R_C = 884\ K\Omega$ $\rightarrow V_{REF} = 0{,}53\ V$

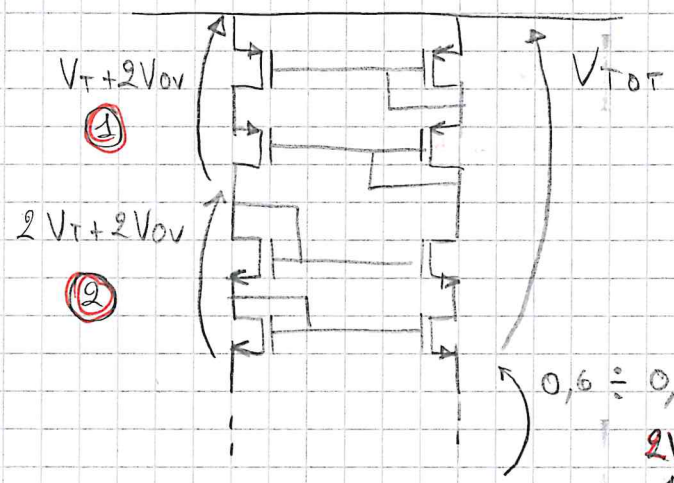
Thanks to the current division we downsized the output voltage. However, we still have all the issues mentioned (Gloop not ∞, mismatch, low β, Z_{OUT}, r_o) ...

47) Power supply rejection using cascoded references and integrated bias generation for the cascodes

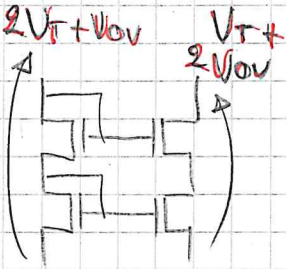
Consider the usual Gloop >∞ ref. $V_{TN} = |V_{Tp}| = V_T$ $V_{ovN} = V_{ovp}$



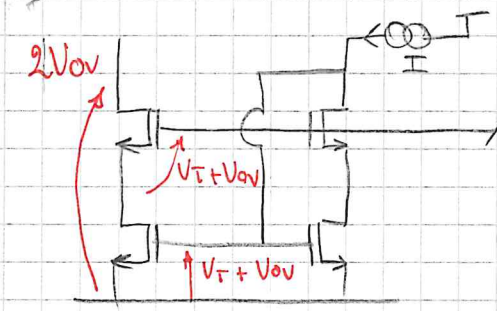
cascode →



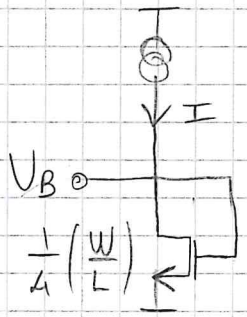
By considering the minimum allowable voltages we get $V_{TOT} = 3V_T + 4V_{ov} = ① + ②$



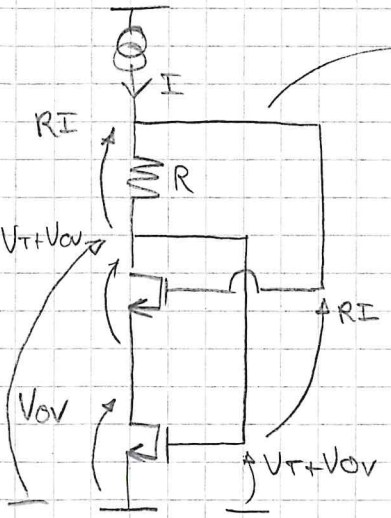
We can get better results with the use of the enhanced mirror:



$V_B = V_T + 2V_{ov}$ →

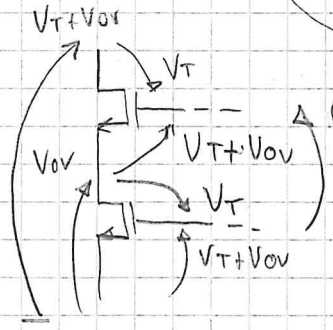


We gain some headroom, however we need to generate V_B and therefore we burn more power, can we integrate V_B directly into the mirror itself? Yes, with the following:

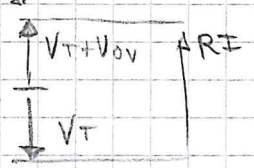


It's easy to see that:

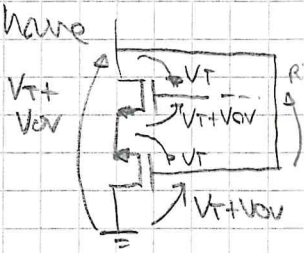
$$RI = V_{ov} = \sqrt{\frac{I}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n}}$$



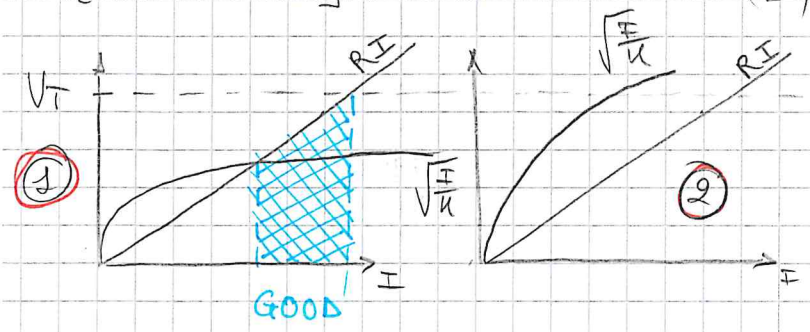
RI →



The ultimate limit will be $RI < V_T$ since we must have $V_T + V_{ov}$ on the sum of the V_{DS} of the MOSFETs:



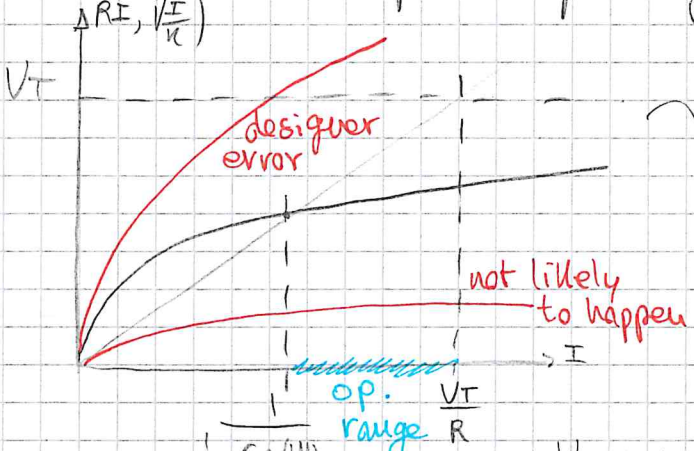
$\left\{ \begin{array}{l} RI < V_T \\ RI = V_{ov} \end{array} \right.$ → We must size $\left(\frac{W}{L}\right)$ and I correctly



① $\sqrt{\frac{I}{K}}$ sized so that it touches RI before V_T

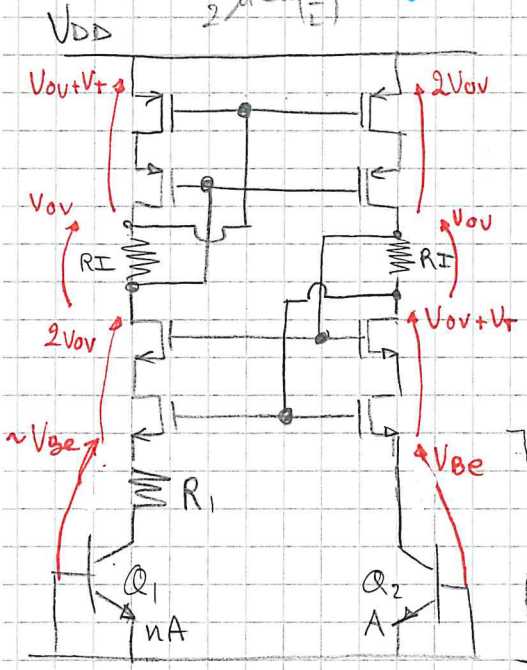
② Badly designed

The needed operating range is $\frac{1}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)R} < I_{OP\ RANGE} < \frac{V_T}{R}$



→ We'll select $I_{op.range}$ so that we get some margin during operation

Let's see the complete cascode circuit. $V_T = V_{Tn} = |V_{Tp}|$, $V_{ov_n} = V_{ov_p} = V_{ov}$



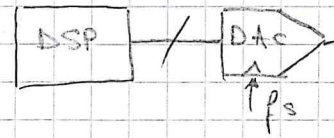
$V_{TOT}|_{MIN} = 4V_{ov} + V_T$ while it was $3V_T + 4V_{ov}$ before. With this implementation we save V_T per each (n,p type) cascode.

In reality, we need to keep a margin for RI because of the before mentioned issues.

→ Pay particular attention where to put the $Q_1 + R_1$ so that we get the $0 < G_{loop} < +1$

This topology is one of the few cases in which transistors are designed to work with higher supplies because of course this circuit cannot work for $V_{DD} \sim 1V$.

48) Data converters introduction



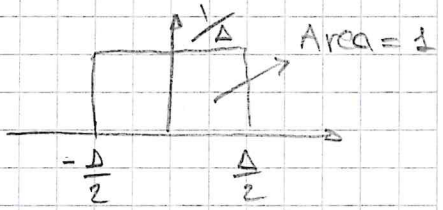
Issues: • Noise • BW of DAC • glitches/errors • settling time • quantization noise

σ_{quant} is the variable that tells us we can't have an accuracy of D/A conversion. Also, the limitation is always analog since it's very difficult to get ~20 bit while digital can reach 64 bit with no difficulty.

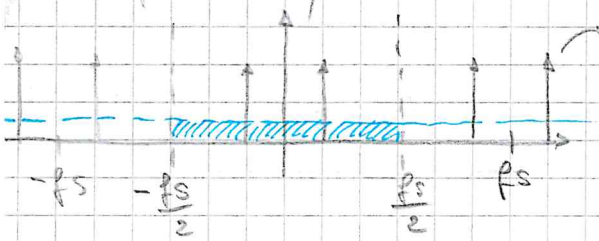
If reproduced signal has HF content, then quant. noise changes rapidly and it can be considered like a white noise.

V_{FS} = full scale range of the DAC

$\Delta = \frac{V_F}{2^B} = LSB$ then $\sigma_\Delta = \frac{LSB^2}{12} = \frac{\Delta^2}{12}$



Since we have quantized signals, the spectrum should be multiplied by a $sinc^2$ but we neglect it for this discussion:



Quantization noise level will be:

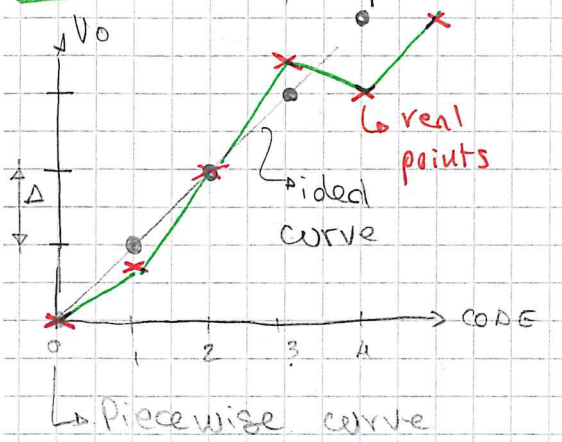
$$S_q = \frac{power}{BW}\left[\frac{V^2}{Hz}\right] = \frac{\Delta^2/12}{\frac{f_s}{2}-\left(-\frac{f_s}{2}\right)} = \frac{\Delta^2/12}{f_s}$$

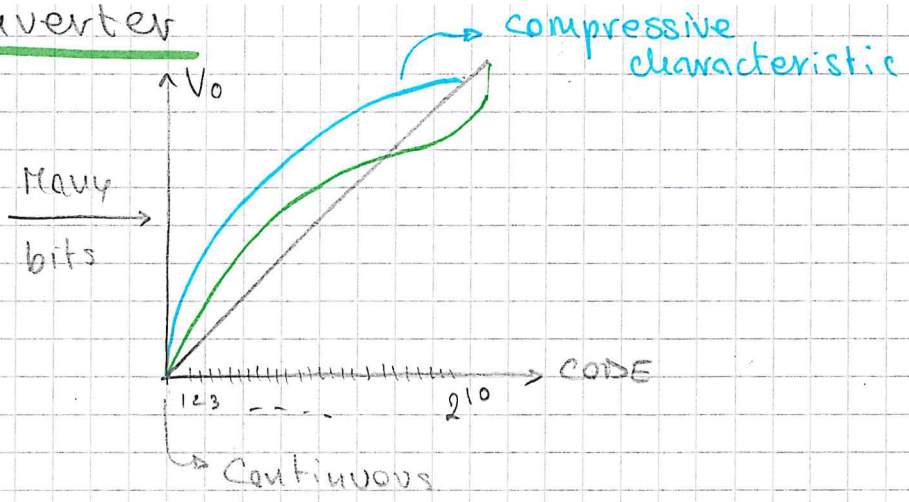
The condition to have an "uncorrelated" quantization noise for a sine wave is: avoid $\frac{f_s}{f_{IN}} = K$ where K = integer or fraction

e.g. if $K = \frac{17}{4} \rightarrow 17\,T_s = 4\,T_{IN}$ ↝ periodicity of quant noise

So K needs to be irrational (which is usually the case since the signal is not just a sine wave)

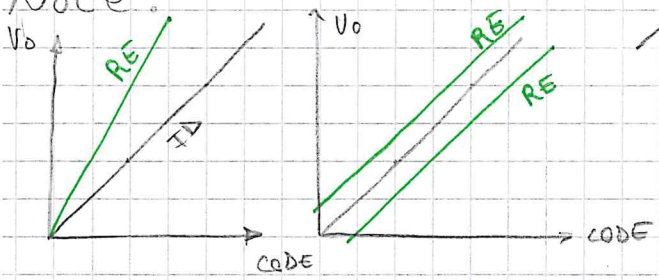
4.9) Linearity of a converter





We have two typical measures: INL, DNL. However these are referred to just the static characteristic, what happens at AC

Note:



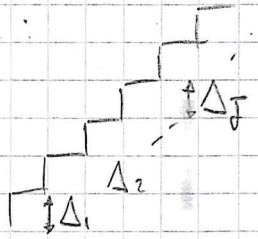
↳ offsets and gain error are still considered linear because they can be easily corrected afterwards.

DNL: Differential Nonlinearity

Def it's the difference between the real step and the average step of the characteristic:

$$\bar{\Delta} = \sum_{i=0}^{N-1} \frac{\Delta_i}{N} \longrightarrow DNL_j = \Delta_j - \bar{\Delta}$$

↳ step index



DNL_j = diff. nonlin. of the j-th step

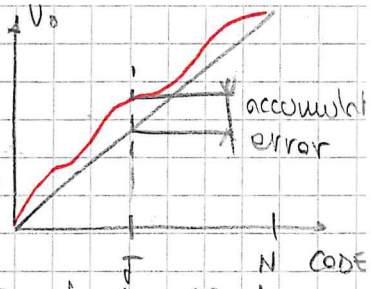
We take the average of the steps as to discard any gain and offsets affecting the conversion.

If we computed $DNL_j = \Delta_j - \Delta_{nominal}$ we would get large DNL error even with a gain error

INL: Integral Nonlinearity

$$INL_J = \sum_{i=0}^{J} DNL_i$$

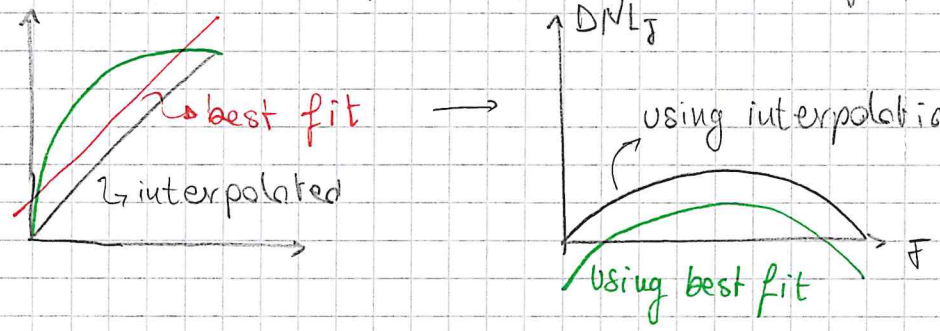
The idea is to compute the accumulated error



of the curve at the J-th step. However, if we just use

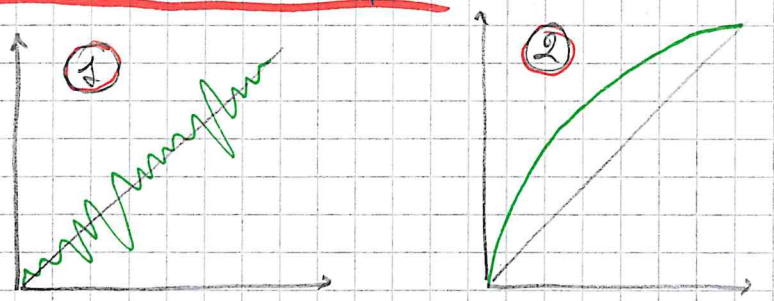
$INL_J = \sum_{i=0}^{J} \Delta i$ ↝ we would end up with large error when the curve is affected by gain / offset errors!

Note: some books study the definition of DNL, INL with either the linear regression of the curve as the avg one (best fit) or just by interpolating the first and last point:



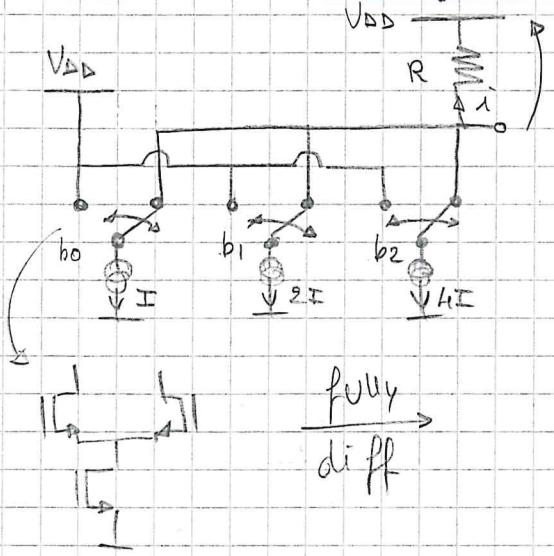
We don't really care, DNL and INL are statistical quantities. We care to use them to get an idea of the linearity.

DNL, INL example



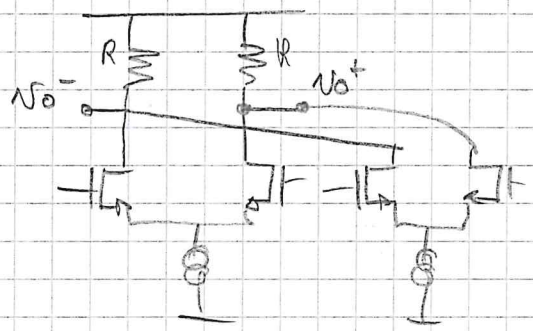
1. Not monothonic, BAD DNL, GOOD INL. Note that monothonicity is critical in cases in which DAC is in a feedback loop (sign changes ⟶ Gloop goes from <0 to >0
2. Monothonic, GOOD DNL, BAD INL

50) Current steering DAC



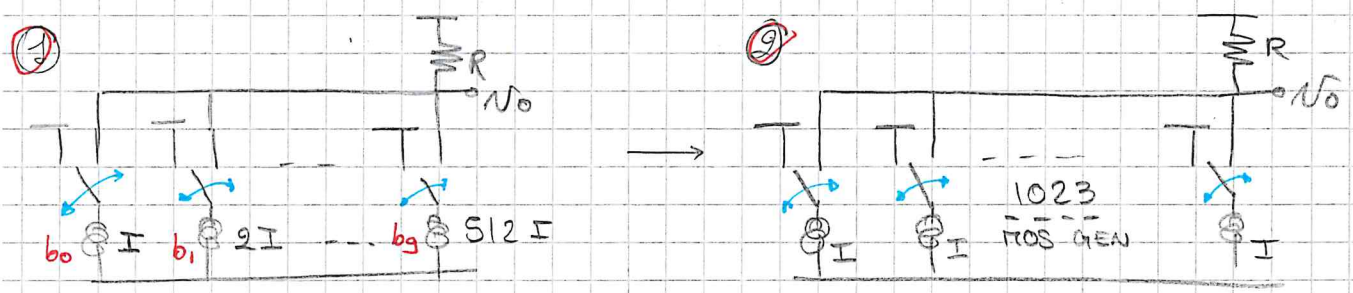
Current flowing into R for a 3 bit DAC is:

000 : I, 001 : 2I, ..., 111 : 7I



We will avoid fully diff DAC in our discussion even though they are the most used

e.g: 10 bit, 500 Msps DAC



binary weighting — thermometric weighting

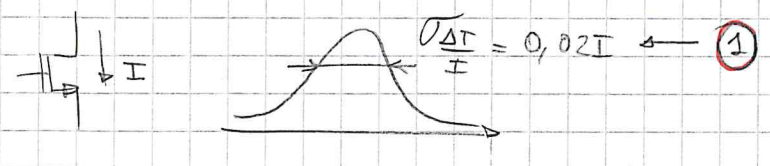
Each current generator is noisy, the LSB one (less current) is the noisier → will be the most critical one for the binary DAC. Thermo DAC have all equal generators

(1) has 10 connection lines
(2) has 1024 connection lines
→ Note that the occupied area of the current gen is the same for both types

(1) Consider the middle characteristic switch (from 511 I to 512 I) → We are turning off $b_0, \dots, b_8$ and turning ON b_9 → high probability of glitching → large error

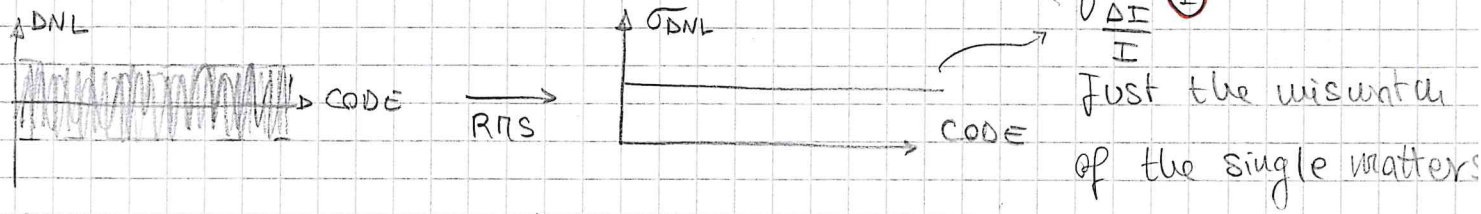
(2) The probability of glitches depends on just the level:
e.g: I want 10 LSBs more → 10 current gen need to switch

5) Current steering DAC: statistical mismatches and DNL / INL



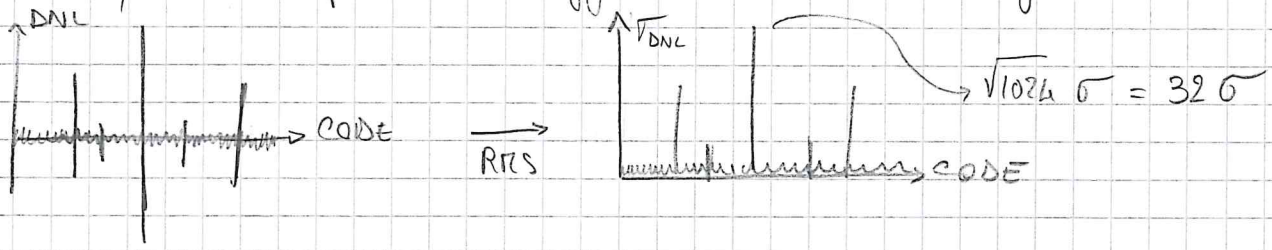
DNL (look at scanned plots): consider 1000 simulations

- Thermometric: just a single current gen is switching each time → DNL should be constant



Just the mismatch of the single matters

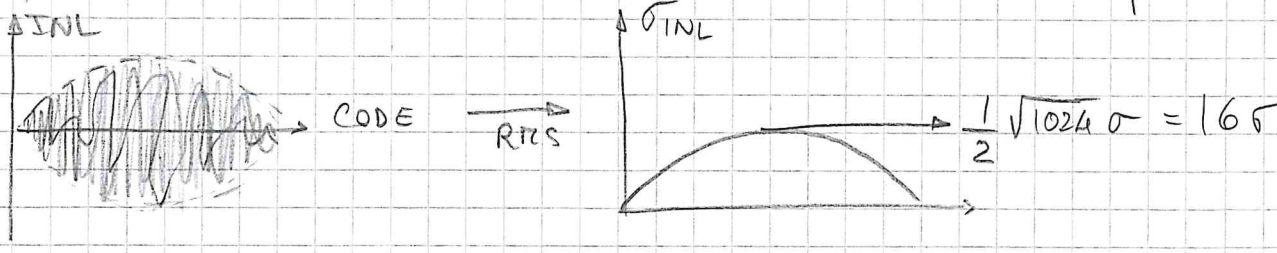
- Binary: we expect the biggest DNL to be right at 511 → 512:



At the peak we end up with a x32 error wrt thermo!

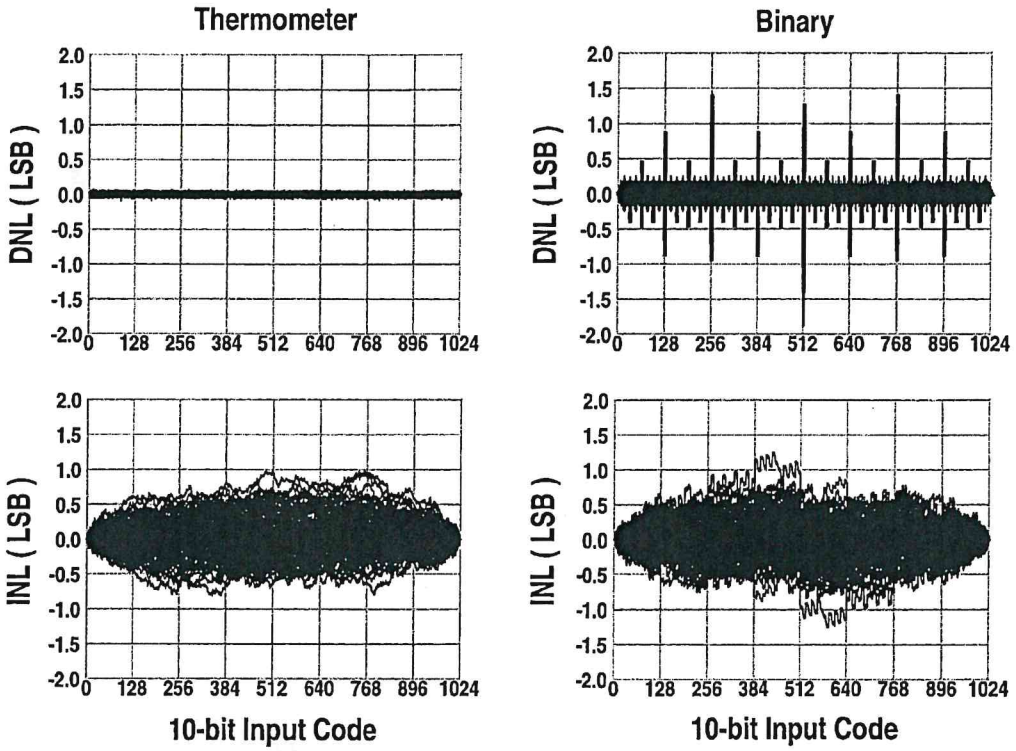
Even though current gen are the same, the switching selection matters a lot when it comes to DNL!

INL: since it is the sum of past error, the only thing that matters is the number of generators (single I), not how they are connected → INL should be the same for thermo/bin

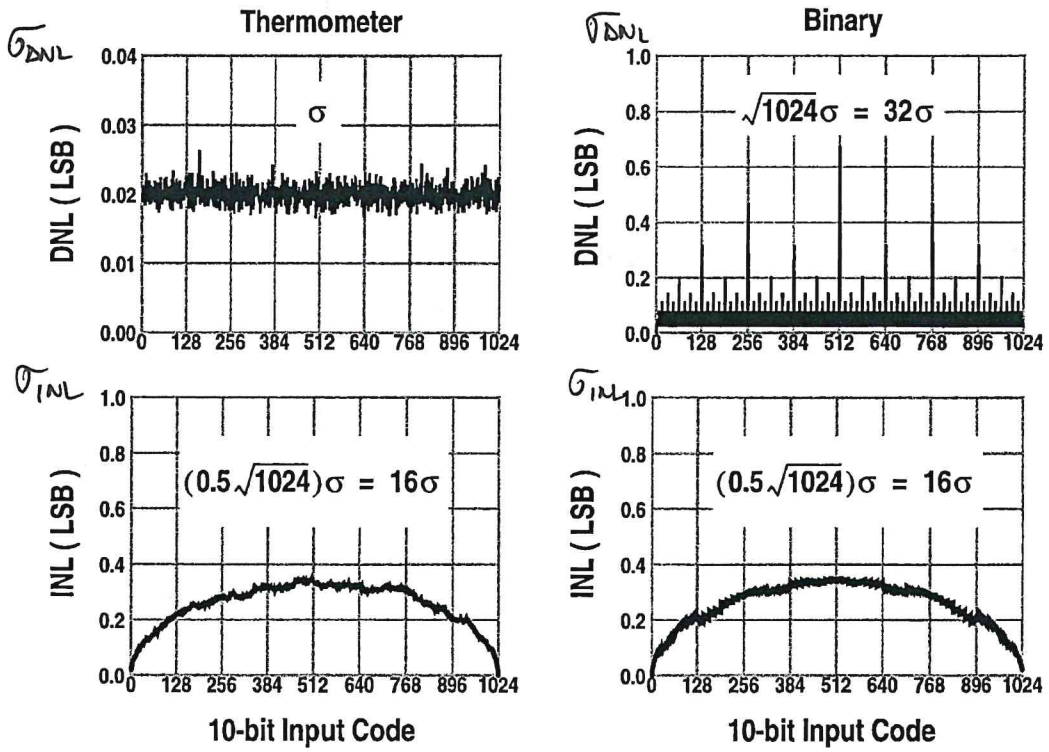


Note that these are statistical quantities, it could happen that one binary DAC is way better than a thermo one!

Source: IEEE Journal of Solid-State Circuits, vol. 33, no.12, Dec. 1998, pp. 1948-1958 (C. Lin, K. Bult)

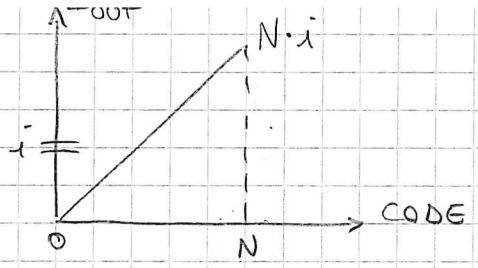


One hundred MATLAB simulation results for thermometer-coded versus binary-weighted DAC.



RMS of 100 MATLAB simulation results for thermometer-coded versus binary-weighted DAC.

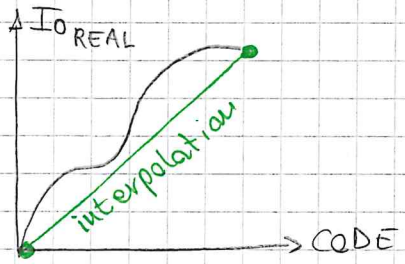
INL rms peak value demonstration



We said that $\sigma_{INL} = \frac{1}{2}\sqrt{1024}\,\sigma = 16\,\sigma$

$I_{OUT}\Big|_{1023} = N \cdot i$ and slope is $SL = \frac{Ni - 0}{N} = i$ → Single step slope (ideal)

Where i is the single current gen value



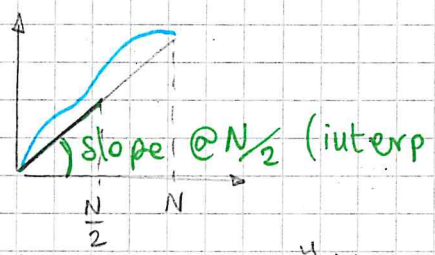
Each step slope is not i, but it will be $i + \delta_J$, where δ_J is the error affecting the LSB step, so

$$SL = \frac{\sum_{J=1}^{N} i + \delta_J}{N} = \frac{Ni + \sum_{J=0}^{N} \delta_J}{N} = i + \frac{1}{N}\sum_{J=0}^{N} \delta_J$$

Since we're interested at the rms INL peak, what's the statistical error in the middle? CODE = N/2 (middle)

@ $\frac{N}{2}$ → real value is $I_0 = \frac{N}{2} i + \sum_{J=0}^{N/2} \delta_J$

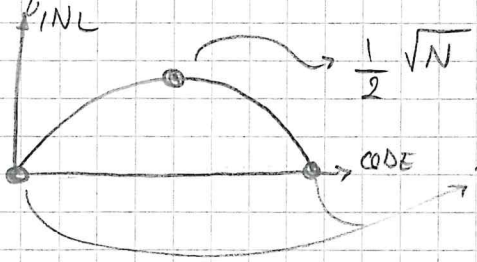
→ interpolated value is $I_0 = \frac{N}{2} i + \frac{1}{2}\sum_{J=0}^{N} \delta_J$



Note: real is taken at $\frac{N}{2}$ while interpolated just uses "the last point" therefore it considers all N

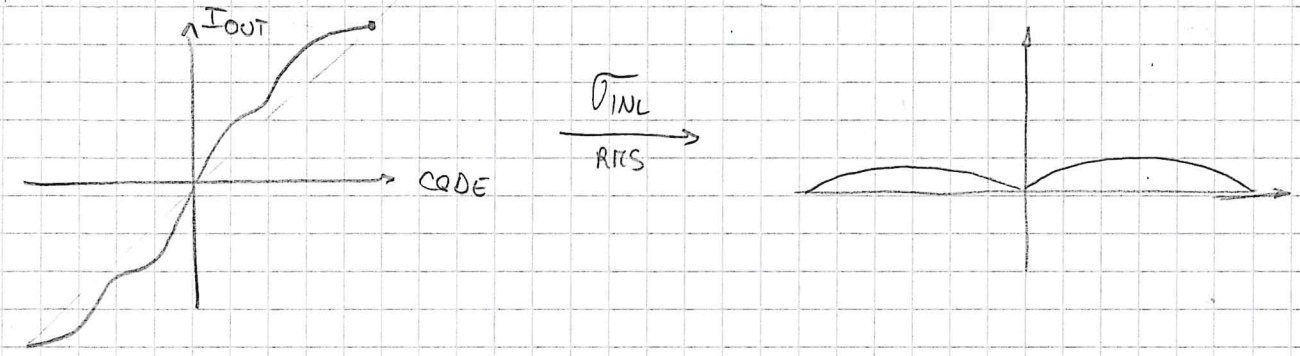
$$ERROR = \sum_{J=0}^{N/2} \delta_J - \frac{1}{2}\sum_{J=0}^{N} \delta_J = \frac{1}{2}\sum_{J=0}^{N/2} \delta_J - \frac{1}{2}\sum_{J=\frac{N}{2}+1}^{N} \delta_J$$

$$\sigma^2 = \frac{1}{4}\frac{N}{2}\sigma_\delta^2 + \frac{1}{4}\sigma_\delta^2 \cdot \frac{N}{2} = \frac{1}{4} N \sigma_\delta^2 \rightarrow \sigma_{INL} = \frac{1}{2}\sqrt{N}\,\sigma_\delta$$



0 error because 1st and last points are the only ones that are perfectly interpolated

Note: for a fully differential DAC, σ_{DNL}, σ_{INL} are symmetrical wrt zero:



So all the DNL, INL analysis + peak value are valid both for single and fully differential topologies!

5.2) Segmentation of current steering DAC

Given a specific DNL_{MAX}, for example 0,5LSB, what would be the needed area for each current generator

- Thermometric → area A
- Binary → area 1024A because of $\sigma^2 \propto \frac{1}{WL} = \frac{1}{A}$ and remember that we're talking about max DNL, which for binary was $\sqrt{1024}\,\frac{\sigma_I}{I}$

However, thermo needs lots of area because of the many connections

Given a specific INL, say 0,5LSB, we would get:

- Thermo → 256 A
- binary → 256 A

→ because of $\frac{1}{2}\sqrt{1024}\,\sigma_I$. INL figures are the same

Very often neither structure is ok. Solution? Segmentation

We split the first LSBs in one type and the MSBs in another

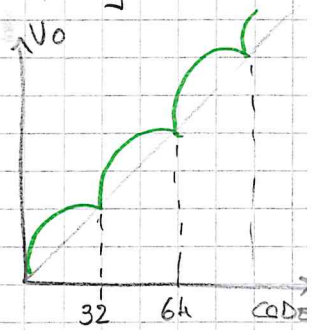
There's no rule on how to do the split:

e.g: first 5 bits → bin — I, 2I, 4I, 8I, 16I → 5 lines

last 5 bits → thermo — 32I, 32I, 32I ---- 32I → 31 lines

Total current is $I_{TOT} = 31\,I + (32 \cdot 31)\,I = 1023\,I$

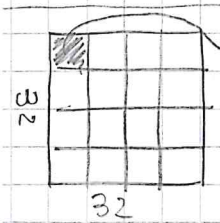
DNL, INL analysis of this is difficult, but output will have some periodicity. For example →



Let's see:

• full bin → 10 lines • full thermo → 1024 lines • segmented → 36 lines

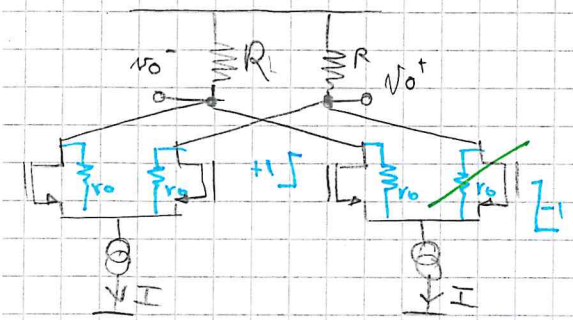
36 is larger than 10 but $\ll 1024$.



→ Area of a current gen → We need to take care of process gradients. How do we choose the positions of the generators? Maybe some centroid placement.

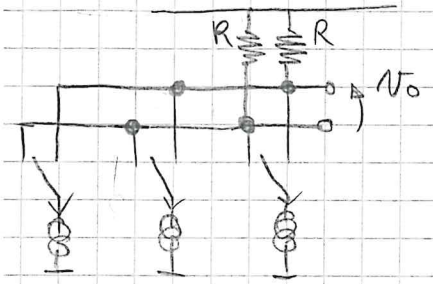
It is also possible to perform dynamic scrambling of the positions of each generator to have better DNL, INL

3rd HD3 effect because of r_o and VDD

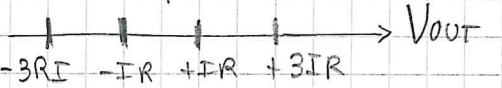


The diff stage is fully unbalanced towards one or the other MOSFET. It follows that load resistors R will see a different r_o for each combination of currents!

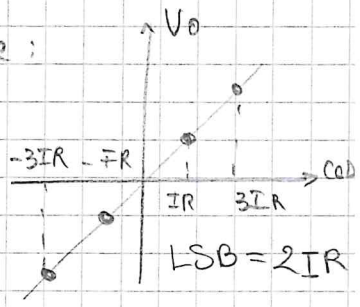
example: 2 bit thermo DAC:



The possible combinations are:



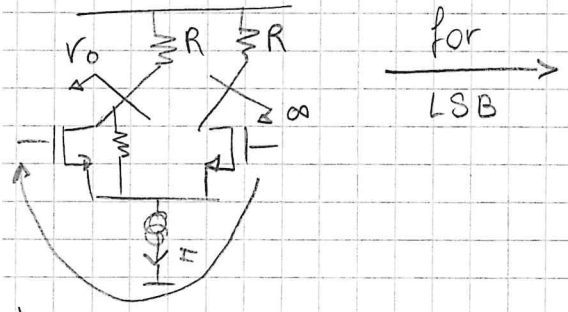
So the static, fully diff characteristic is →



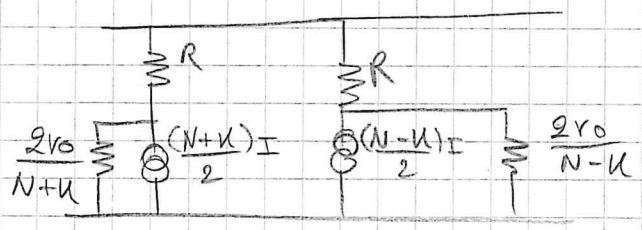
10 bit r_o study

Let's call CODE as index K, so $N = 1023 \Rightarrow -N < K < +N$

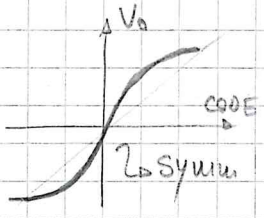
We said that the total resistance seen by R (load) changes with K:



for LSB →



Note: this is systematic, and since it's symmetrical because it's fully differential → 3rd harmonic generation!



$$V_{OUT}(K) = \frac{I(N+K)}{2} \cdot \frac{R \cdot \frac{2r_o}{N+K}}{R + \frac{2r_o}{N+K}} - I\frac{(N-K)}{2} \cdot \frac{R \cdot \frac{2r_o}{N-K}}{R + \frac{2r_o}{N-K}} =$$

$$= \cdots \Rightarrow V_{OUT}[K] \underset{r_o \gg NR_L}{\cong} IRN\left[\left(\frac{K}{N}\right) + \left(\frac{K}{N}\right)^3 \left(\frac{NR}{2r_o}\right)^2\right]$$

if $r_o \gg NR_L$

↳ linear ↳ 3rd harmonic

Note: if N is large and $R_L \sim 50\,\Omega$, it's hard to meet the $r_o \gg NR_L$ requirement. If this is not met, we will see additional, odd harmonics term in $V_{OUT}[K]$

$$V_{OUT}[k] \cong IRN\left[\left(\frac{k}{N}\right) + \left(\frac{k}{N}\right)\left(\frac{NR}{2r_o}\right)\right]$$

$$V_{OUT}[x] \cong G\left[x\alpha_1 + \alpha_3 x^3\right]$$

G → const. gain; $x\alpha_1$ → lin term; $\alpha_3 x^3$ → 3rd ↝ general expression for a 3rd ord distortion gain stage

$G = IRN$, $\frac{k}{N}$ = normalized input → $-1 \le \frac{k}{N} \le +1$, $\alpha_3 = \left(\frac{NR}{2r_o}\right)^2$, $\alpha_1 = 1$

For a sinusoid $V_{OUT} = A\sin(\omega t)$ we get:

$HD_3 = \frac{1}{4}\frac{\alpha_3}{\alpha_1}A^2$, if $A = 1$ (maximum output), then $HD_3 \cong \left(\frac{N}{4}\frac{R_L}{r_o}\right)^2$

e.g: requirement is $HD_3 < -60dB \rightarrow 4r_o > \sqrt{10^3}NR$

Note: $r_o \to \infty$ then $HD_3 = 0$ of course

V_{DD} effect on HD_3

$$V_{OUT}\Big|_{V_{DD}}(k) = V_{DD}\cdot\frac{\frac{2r_o}{N-k}}{R+\frac{2r_o}{N-k}} - V_{DD}\frac{\frac{2r_o}{N+k}}{R+\frac{2r_o}{N+k}} \Rightarrow \text{assume } r_o \gg NR \Rightarrow$$

$$V_{OUT}[k] \cong V_{DD}\frac{RN}{r_o}\left[\left(\frac{k}{N}\right) + \left(\frac{k}{N}\right)^3\left(\frac{NR}{2r_o}\right)^2\right]$$

Same expression of r_o effect, but G is different.

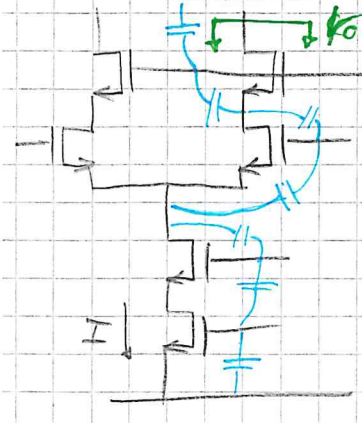
Typically $IRN \gg V_{DD}\frac{RN}{r_o}$ → $Ir_o \gg V_{DD}$ → $V_A' \gg 1,2V$

(V_A': $V_{DD} \sim 1,2$ typ; V_A' confirmed)

For this reason, V_{DD} effect is usually neglected

(also, V_A is the one of a cascoded generator → even larger)

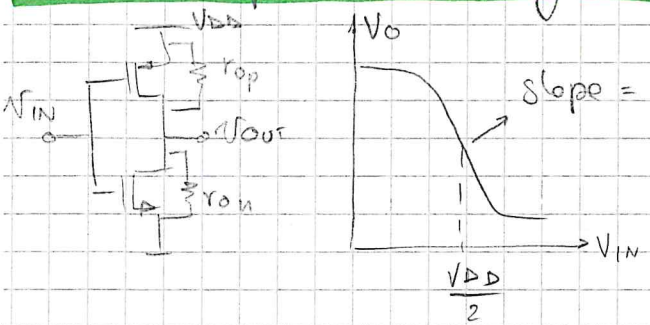
Effect of Cpar



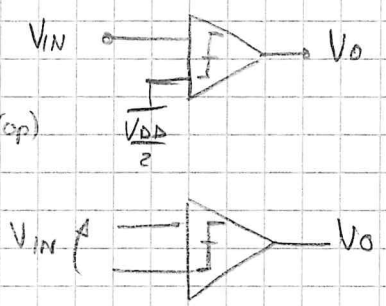
↝ In the real implementation we find multiple cascodes. With larger frequency, all Cpar start to short, therefore r_o value continues to decrease and HD_3 increases.

The $V_{OUT}[k]\Big|_{r_o}$ formula is in fact valid for DC only

5.4 / Comparator design: latch

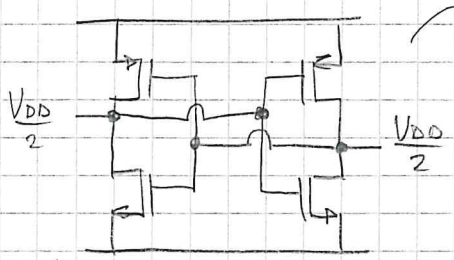


$$slope = (g_{m_n} + g_{m_p})(r_{on} \,//\, r_{op})$$



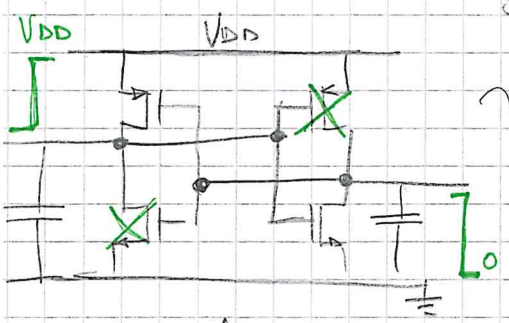
We could use an inverter to have a well defined output (1/0). But we need a threshold and an opamp is too complex. What can we do

Positive feedback and simple latch



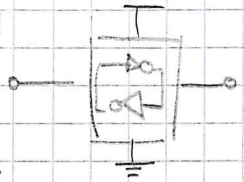
↳ initial condition, left and right out are $\sim \frac{V_{DD}}{2}$

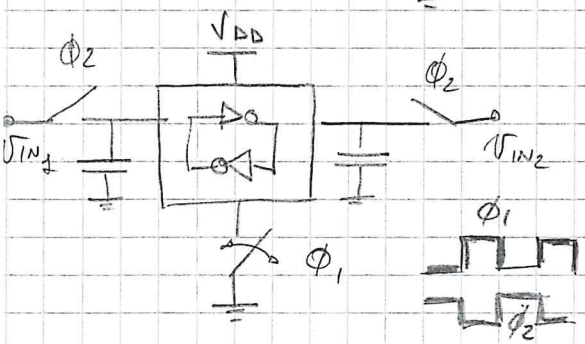
Suppose $\mu_p \left(\frac{W}{L}\right)_p = \mu_n \left(\frac{W}{L}\right)_n$ → because of positive feedback we can't have a $\frac{V_{DD}}{2}$ stable point:



↳ We need to exploit this to be used as a comparator

Simplify the schematic →

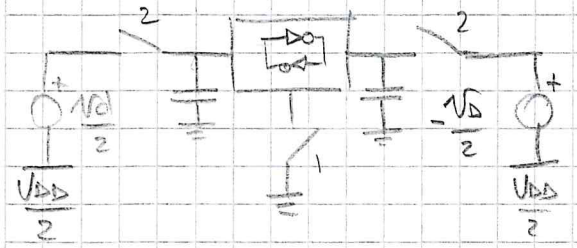




ϕ_1: latch is off and capacitors are connected to V_{IN}

ϕ_2: latch is on and circuit unbalances based on capacitor voltage condition.

Since we have a very small V_{IN}, capacitors will be just slightly unbalanced ($\sim$ 1mV input)



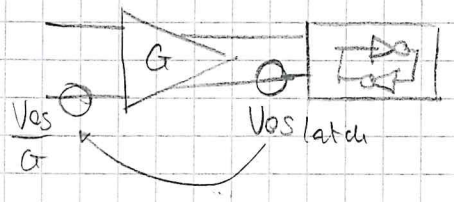
A complicate problem is T_{CK} selection. If V_{IN} is too small, time for regeneration (ϕ_1) could be not enough → metastability issues.

Note:

- noise has to be smaller than V_{IN}
- V_{OS} has to be smaller than V_{IN}
- charge injection of the switches must be less than V_{IN}

issue: because of the hard switching we risk of injecting hard disturbances to the source → Kickback

We put a preamp in order to have better reverse isolation to the source (imagine a 16 bit flash → 16 comparators)

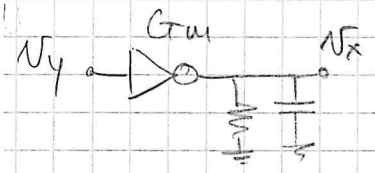


The preamplifier can also be used to relax some parameters (e.g: noise)

Note: since we have both preamp and latch implemented with the same technology, preamp will show the same Vos. However, this Vos can be removed with some techniques (e.g: CDS).

Offset requirements can be critical in pipelined / interleaved architectures

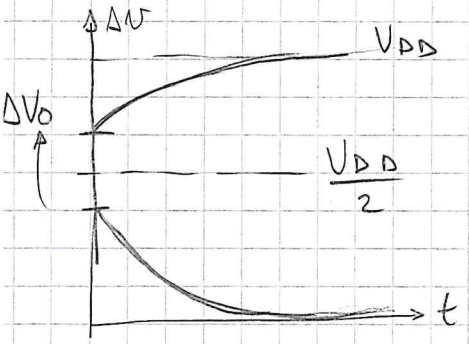
Latch speed: we want to study the speed of the device



$$\begin{cases} Gm\,V_y = -\frac{V_x}{R} - \left(\frac{dV_x}{dt}\right)C & \rightarrow \text{inv 1} \\ Gm\,V_x = -\frac{V_y}{R} - \left(\frac{dV_y}{dt}\right)C & \rightarrow \text{inv 2} \end{cases}$$

Define $A_v = Gm\,R$ → gain, $\Delta V = V_x - V_y$ → if we simplify the equations

$$\tau\,\frac{d[\Delta V]}{dt} = \Delta V[A_v - 1] \rightarrow \Delta V = \Delta V_0\, e^{\left(\frac{A_v-1}{\tau}\right)t}$$

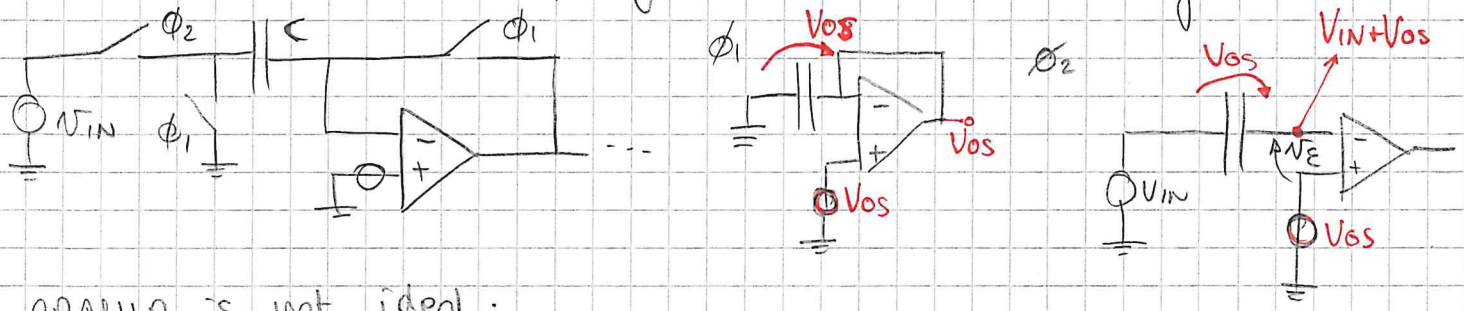


Metastability occurs when ΔV_0 is too small → V_x, V_y lock to $V_{DD}/2$ for a long time. This is complicated to study and we'd just discard the data anyway (because it's not a clear 1/0 VDD/gnd).

We won't study metastability because offset/noise/power are well worse of a problem wrt metastability.

3.3) Offset reduction and canceling on latches + preamp

Correlated Double Sampling (CDS) or autozeroing:

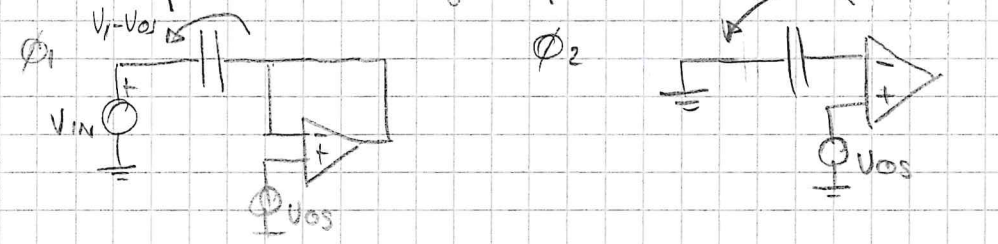


If opamp is not ideal:

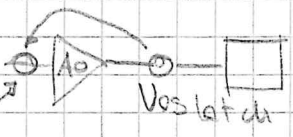
$$V_C\Big|_{\phi_1} = V_{OS}\frac{A_0}{1+A_0} \qquad V_{IN}^-\Big|_{\phi_2} = V_{IN} + V_{OS}\left[\frac{A_0}{1+A_0}\right] \rightarrow V_\varepsilon = V_{IN} + \frac{V_{OS}}{1+A_0}$$

Note that the preamp has $A_0 \sim 10 \div 20$ so

What if we change phases? $V_{IN}-V_{OS}$ It still works but now on ϕ_1 V_{IN} needs to drive the amplifier and capacitor!



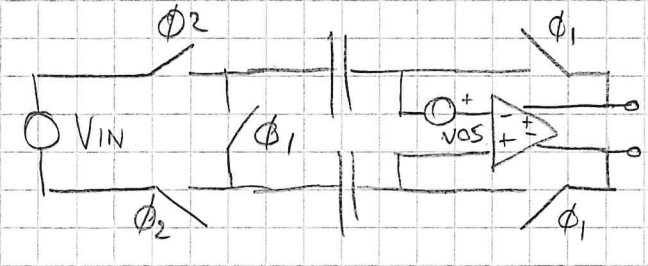
So now $V_{OS}\Big|_{TOT} = \frac{V_{OS\,PREAMP}}{1+A_0} + \frac{V_{OS\,LATCH}}{A_0}$



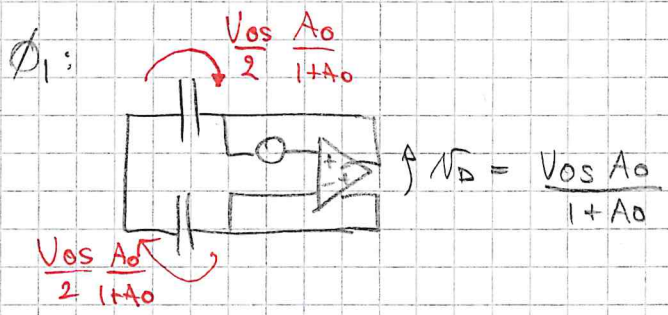
Be careful: noise doubles because of the CDS.

We also expect this to partially cancel 1/f noise (see CDS notes on Signal Recovery)

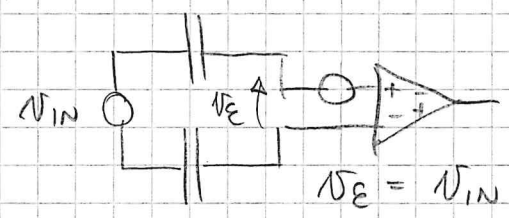
Fully diff CDS



ϕ_1:



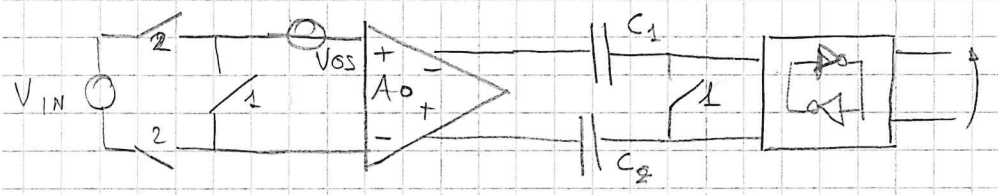
ϕ_2



$$V_\varepsilon = V_{IN} - \frac{V_{OS}}{1+A_0}$$

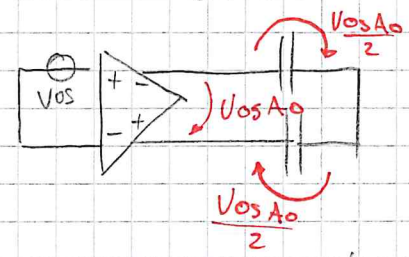
Output offset canceling

Since $A_0 \sim 10 \div 20$, CDS will attenuate V_{OS} by $\frac{1}{1+A_0}$ but it will not cancel it. Also this Output Offset canceling (OOS) can be considered to be a CDS but it focusses on sampling the output offset directly:

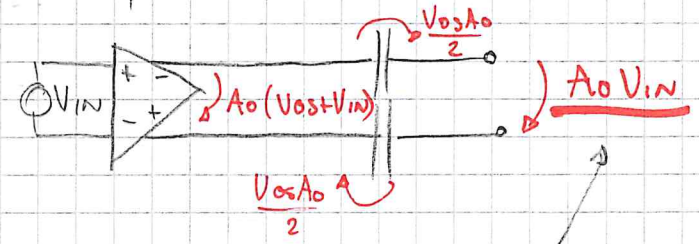


Note: $C_1 = C_2 = C$ but what matters is the total branch voltage so $C_1 \neq C_2$ does not generate any mismatch issue in OOS

ϕ_1



ϕ_2

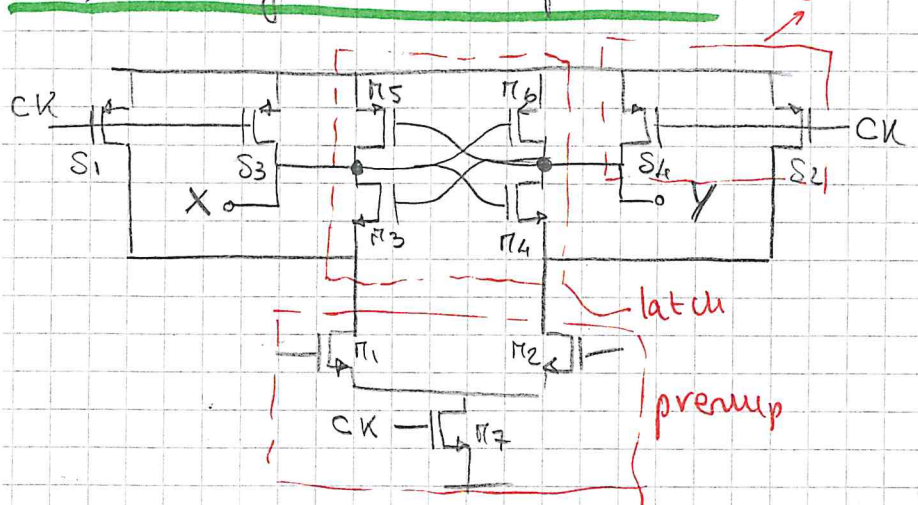


We see that in ϕ_2 we don't get any offset

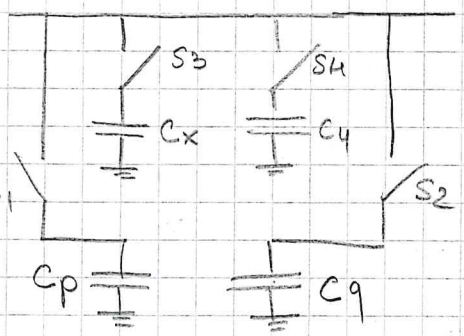
However, this is not used because AC coupling does not let us easily set common mode voltages when we have to switch between two different levels.

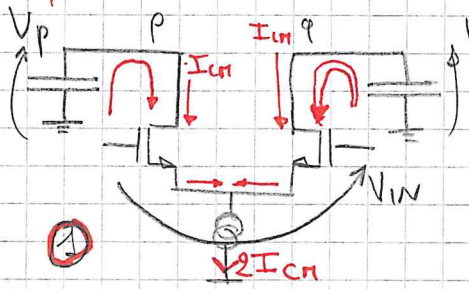
Moreover, preamp is usually embedded into the latch

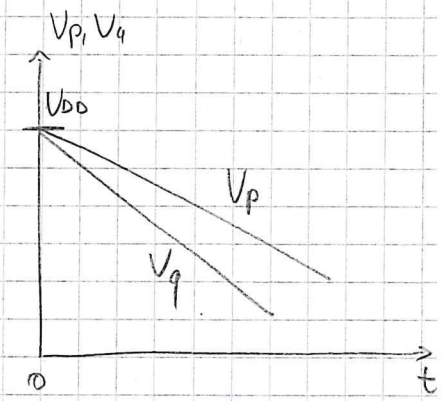
56) Strong arm comparator



CK is just a sync signal. For M_7 it opens/closes, while for S_{1234} it shorts the signal to V_{DD}







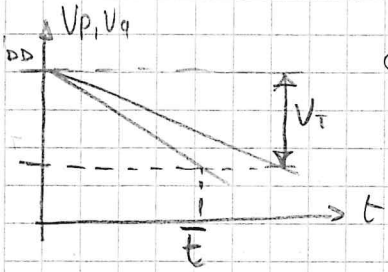
At time 0^-, C_p and C_q are at V_{DD}, shorted by switches S_1, S_2. C_x and C_y are connected to V_{DD} as well → M_3 and M_4 drain and gate are shorted to V_{DD} → $V_G = V_D = V_S\big|_{M_3,M_4} = V_{DD}$

At time 0^+, S_1 and S_2 disconnect C_p, C_q leading to (1).

We have a total $I_{cp} + I_{cq} \simeq 2I_{cm} = I_{M7}$ that is discharging C_p, C_q.

Since V_{IN} is more positive towards M_2, V_q will drop faster.

At time $\bar{t}$ one of the two capacitor voltages (V_q in our case) dropped low enough to reach V_T difference ($V_{DD} - V_q\big|_{t=\bar{t}} = V_T$). This means that



M_4 source dropped a V_T under the gate → ON

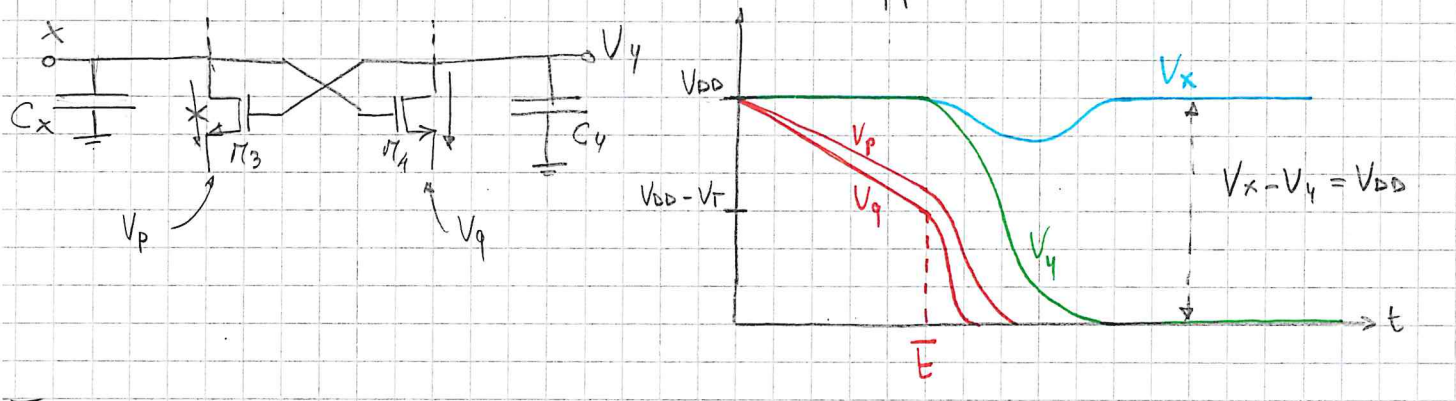
Since $\frac{I_{cm}}{C_{p,q}}\bar{t} = V_T$ → $\bar{t} = \frac{C_{p,q} V_T}{I_{cm}}$ ↳ time for $M_{3,4}$ turn ON

We now want to compute a kind of gain for the preamp:

$$A_V = \frac{|V_p - V_q|}{|V_{IN}|} = \frac{g_{m12}}{C_{p,q}} \cdot \frac{C_{p,q}}{I_{cm}} V_T = \frac{g_{m12}}{I_{cm}} V_T = \frac{2\frac{I_{M7}}{2}}{\frac{I_{M7}}{2} V_{OV}} V_T = \frac{2V_T}{V_{OV}}$$

Note: since V_{IN} is small, the current unbalance can be considered to be small as well. This is why we don't take into account the V_{IN} unbalance for $\bar{t}$ but we consider V_q, V_p to decrease as if they had the same Icm

- At time $\bar{t}^+$, S_3, S_4 open in order to activate the latch. Since now M_4 is ON and M_3 is off:



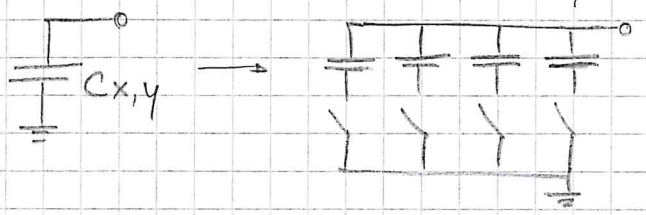
The regeneration starts. Since M_4 is ON it can suck the current and while the output V_y go to zero. Viceversa for M_3.

After some regeneration time $t_{REG} = \frac{C_{xy}}{g_{m3,4}\left(1-\frac{C_{x4}}{C_{pq}}\right)}$ (Not discussed)

V_x and V_y will be either at 0 or V_{DD}.

Note: • after regeneration, $M_{3,4}$ are OFF → blocking state from latch to output → helpful for kickback

- After t_{REG} no power is dissipated → $P_{DISS} = f_{cu} V_{DD}^2 [2C_{pq} + C_{xy}]$
  Both C_p and C_q are charged/discharged; only C_x or C_y are charged/dis. per each clock cycle
- Offset of the whole circuit is corrected on chip by capacitor banks and switches:



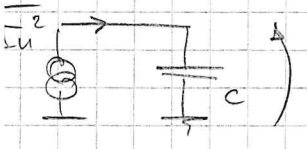
→ capacitors are in thermo/binary weights.

At startup we short V_{IN} and compensate V_{OS}

57) Comparator noise

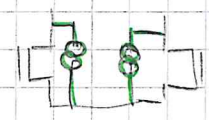
Between 0 and $\bar{t}$ noise affects the strong arm latch on $C_{p,1}, C_{p,2}$.

$$\bar{t} = \frac{C_{p,1} V_T}{I_{D1}} = \frac{2C_{p1} V_T}{I_{D7}}$$



$\overline{i_n^2} \rightarrow$ C $\quad \overline{\sigma_V^2} = \frac{\overline{i_n^2} t}{C}$ ↝ it's a sort of noise integration

We can say that the variance of the out is grossly



$$\overline{\sigma_{p,1}^2} \propto 2 \frac{4kT\gamma g_{m12}}{C_{p,1}^2} t \longrightarrow \overline{\sigma_{p,1}^2}\Big|_{t=\bar{t}} \propto \frac{8kT\gamma g_{m12}}{C_{p1}^2} \frac{V_T C_{p1}}{I_{D1}}$$

$[V^2]$ ↳ grossly estimated

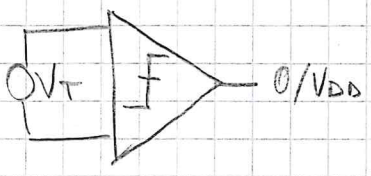
Given $A_V = \frac{g_{m12} V_T}{I_{D1}}$ let's input refer $\overline{\sigma_{IN,V}^2} = \overline{\sigma_{p1V}^2} \cdot \frac{1}{A_V^2} = \frac{8kT\gamma}{C_{p1}} \frac{I_{D1}}{(g_{m12} V_T)}$

Since $\frac{2I}{V_{OV}} = g_{m12} \longrightarrow \overline{\sigma_{IN,V}^2} = \frac{4kT\gamma}{C_{p1}} \frac{V_{OV}}{V_T}$

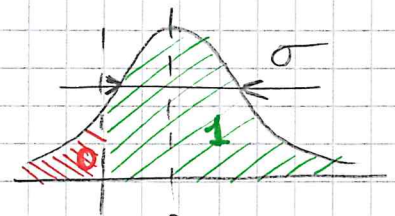
Moreover, given the additional S_1, S_2 kT/C noise:

$$\overline{\sigma_{IN,V}^2} = \frac{4kT}{C_{p1}} \cdot \frac{V_{OV12}}{V_T} + \frac{kT}{2C_{p1}} \frac{V_{OV12}^2}{V_T^2} \rightarrow \frac{kT}{C} \cdot \frac{1}{A_V^2}$$

How do we test a comparator noise? We have 0 and 1 as out:



We apply a small known input bias V_T ⟶



Since noise is 0 mean, by shifting the input by V_T we unbalance the probability of 1 wrt 0

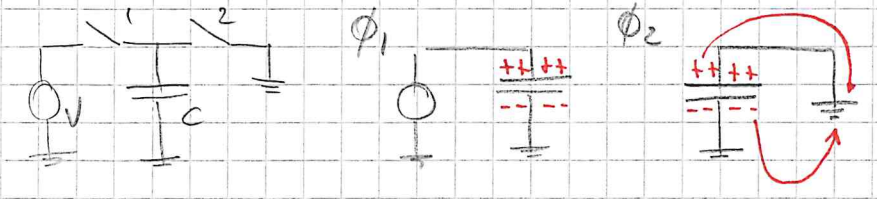
This way we can count #zeros and #ones so that:

$$\frac{n_0}{n_1} = \frac{\int_{-\infty}^{-V_T} f(x)\,dx}{1 - \int_{-\infty}^{-V_T} f(x)\,dx}$$

↳ because of zero bias

If we didn't use V_T, we would get zero mean ($\frac{1}{2}$ probability) and therefore no meaningful result about σ can be obtained!

58) Recall on SW capacitors



$$I_{AVG} = \frac{CV_{IN}}{T_{CK}} = \frac{V_{IN}}{R_{EQ}}$$

$$R_{EQ} = \frac{1}{f_{CK} \cdot C}$$

conservative

On avg we're wasting charge to gnd → since it's not a reversible world we're dissipating power → 0° phase shift (unlike linear capacitors). Few remarks:

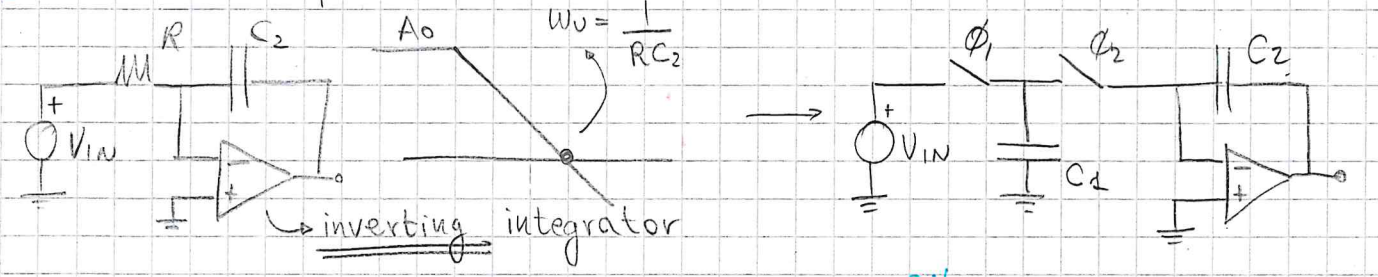
- We can design extremely large resistor values
- We can design filters which cutoff frequency and Q factor ($\tau_{filter} = R_{EQ} \cdot C_2 = \frac{C_2}{C_1 f_{CK}}$) depend only on frequency of the clock (very accurate) and on the relative matching between physical components $\left(\frac{C_2}{C_1}\right)$

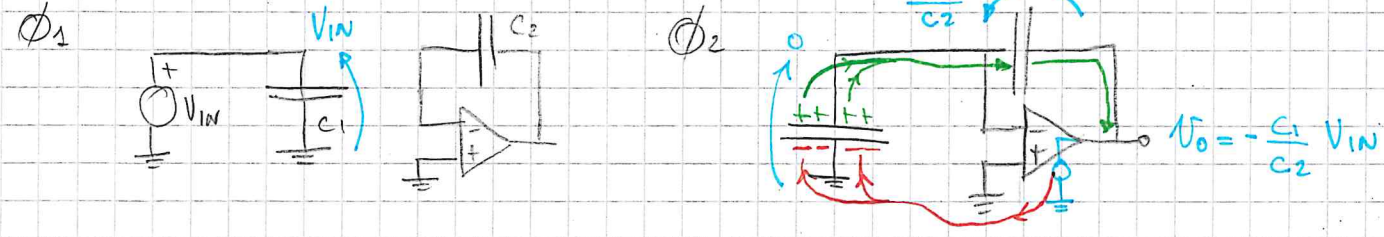
Noise of sw. cap is $4KTR_{EQ} = 4 \left[\frac{KT}{C}\right] \cdot \left[\frac{1}{f_{CK}}\right] \rightarrow \left[\frac{V^2}{Hz}\right]$ ($\left[V^2\right]$, $\left[\frac{1}{Hz}\right]$)

Noise makes sense dimensionally

- Non-inverting integrator topologies come basically for free
- It's very difficult to design single ended stages

3.2) SW cap filter





Check the opamp stability:

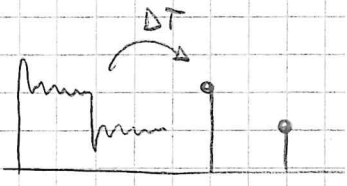
Φ_1: opamp is basically a buffer → we set C_{miller} for the compensation.

Φ_2: C_1, C_2 feedback will narrow the BW if we keep the same compensation used for Φ_1. It seems that we have an overcompensated opamp in Φ_2 and the price to pay is in terms of $t_{settling}$.

In principle, if $\frac{C_1}{C_2} = 2$, we could achieve $BW|_2 = 2\,BW|_1$

Some configurations in fact, during phase 2 remove a part of the Miller capacitor because of the less compensation needed

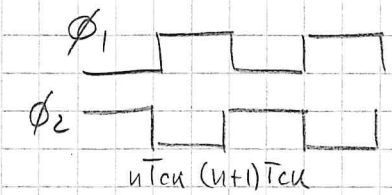
Discrete transfer function computation:



Remember that the z-transform is a model that does not take into account noise / tsettling / ...

We are still working with analog continuous time signals.

Consider the phases:



$$C_2\{V_0[nT_{ck}] - V_0[(n-1)T_{ck}]\} = -C_1 V_{IN}[(n-1)T_{ck}]$$

z-transform

$$C_2 V_0 (1 - z^{-1}) = -C_1 V_{IN} z^{-1}$$

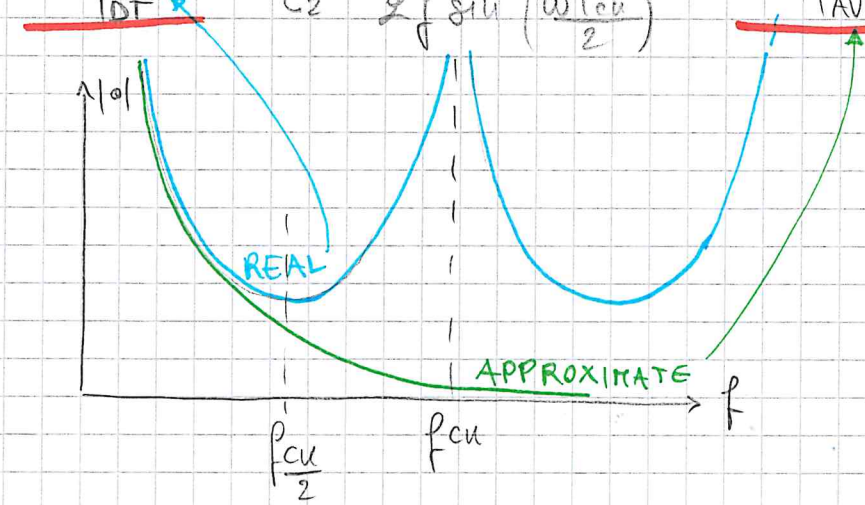
$$\frac{V_0}{V_{IN}}\left(z = e^{+j\omega T_{ck}}\right) = -\frac{C_1}{C_2}\frac{e^{-j\omega T_{ck}}}{1 - e^{-j\omega T_{ck}}} = -\frac{C_1}{C_2}\frac{1}{e^{-j\omega\frac{T_{ck}}{2}}}\frac{e^{-j\omega T_{ck}}}{e^{+j\omega\frac{T_{ck}}{2}} - e^{-j\omega\frac{T_{ck}}{2}}} =$$

$$\frac{V_0}{V_{IN}}(\omega) = -\frac{C_1}{C_2}\cdot\frac{e^{-j\omega\frac{T_{ck}}{2}}}{2j\sin\left(\omega\frac{T_{ck}}{2}\right)}$$

Let us compare the sampled TF and the average Laplace one:

① $TF|_{DT}(\omega) = -\frac{C_1}{C_2} \frac{e^{-j\omega\frac{T_{CH}}{2}}}{2j \sin\left(\frac{\omega T_{CH}}{2}\right)}$

② $TF|_{AVG}(\omega) = \frac{-1}{SR_{eq}C_2} = -\frac{C_1}{C_2} \cdot \frac{1}{j\omega T_{CH}}$



We can clearly see that for $f \ll f_{CH}$ → DT and AVG are the same:

$TF|_{DT}(\omega) = -\frac{C_1}{C_2} \frac{e^{-j\omega\frac{T_{CH}}{2}}}{2j \sin\left(\frac{\omega T_{CH}}{2}\right)} \sim -\frac{C_1}{C_2} \frac{1}{2j\frac{\omega T_{CH}}{2}}$ → same of $TF|_{AVG}$

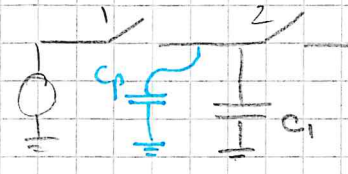
($\omega\frac{T_{CH}}{2} \to 0$; $e^{-j\omega\frac{T_{CH}}{2}} \to 1$; $\sin\left(\frac{\omega T_{CH}}{2}\right) \sim \frac{\omega T_{CH}}{2}$)

While near $\frac{f_{CH}}{2}$ and for larger f → $TF|_{DT} \neq TF|_{AVG}$

In general → if $BW_{filter} \ll \frac{f_{CH}}{2}$ → use ②

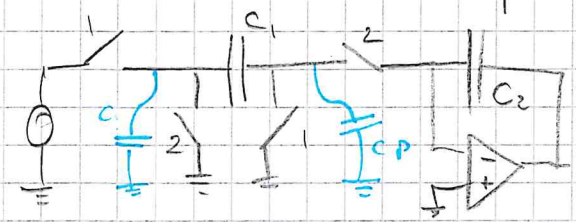
if $BW_{filter} \to \frac{f_{CH}}{2}$ → use ①

60) Parasitic capacitances in SW cap, insensitive topologies

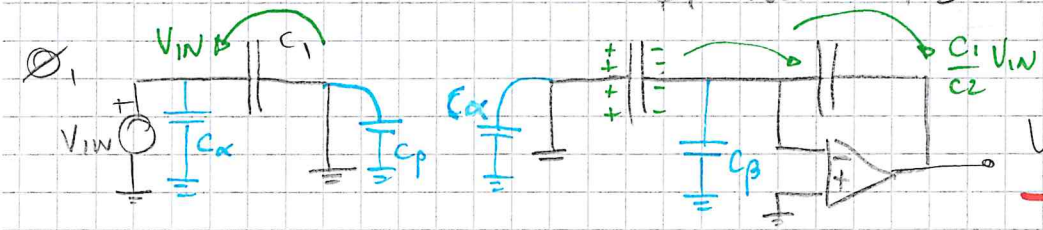


Because of the not controllable value of C_p, we risk some serious deficiencies when designing sw. cap filters.

There are some topologies that mitigate this problem.



We now have two C_p, but let us analyze what happens in ϕ_1 and ϕ_2:



$$V_o = \frac{C_1}{C_2} V_{IN}$$

C_α: @ ϕ_1 it's charged by V_{IN}, @ ϕ_2 it's discharged to gnd

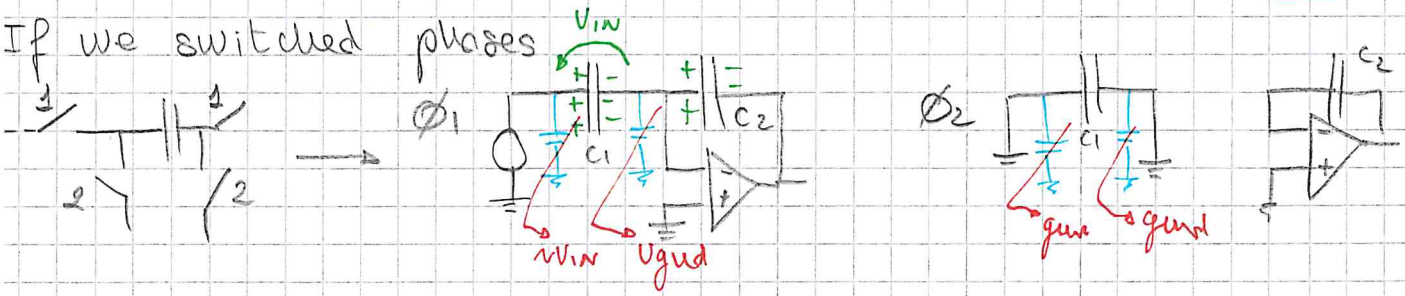
C_p: @ ϕ_1 shorted to gnd, @ ϕ_2 shorted to virtual gnd but it was already discharged in ϕ_1

It's clear that neither C_p contribute to V_{OUT}

Also note that V_o is a non inverting integrator.

The relative z-transform TF is $\frac{V_{OUT}}{V_{IN}}(z) = \frac{C_1}{C_2} \frac{z^{-1}}{1-z^{-1}}$ (1)

If we switched phases



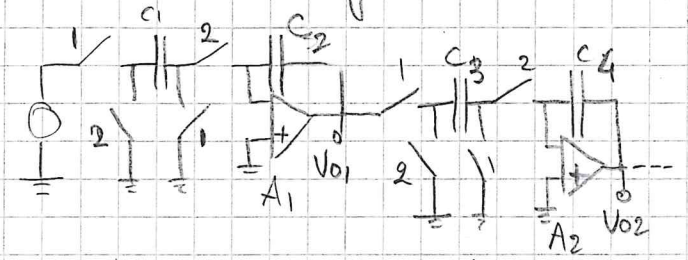
During ϕ_1 $\frac{V_o}{V_i} = -\frac{C_1}{C_2}$

$$\frac{V_o}{V_{IN}}(z) = -\frac{C_1}{C_2} \cdot \frac{1}{1-z^{-1}}$$ ⇝ inverting integrator

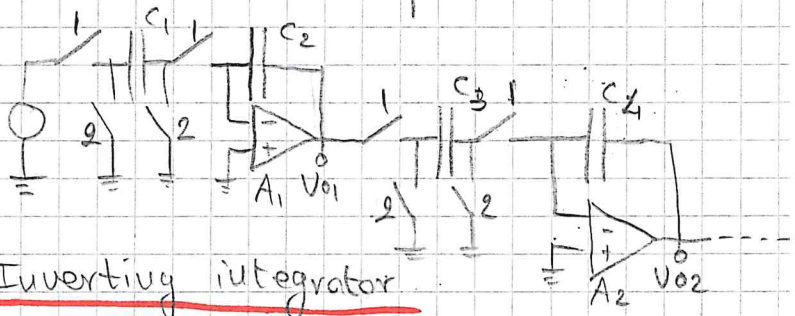
Note that compared to (1), this TF does not have a pure delay at the numerator because V_o is readily available at ϕ_1 (because of the switching order)

61) SW phase order and settling time criticality

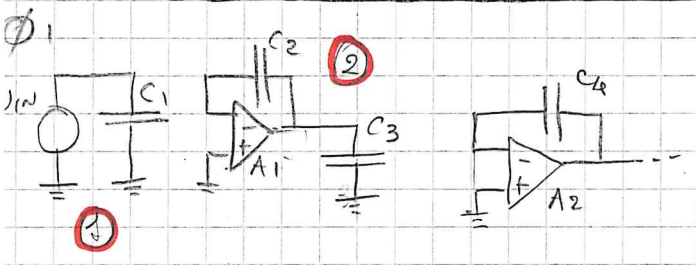
Consider the two stray insensitive topologies. The obvious difference is the sign and the pure delay, but a critical aspect is the settling time. Consider a 7-th order filter:

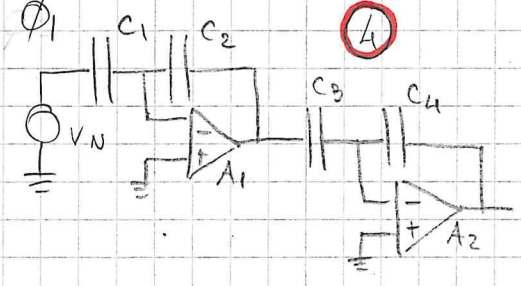


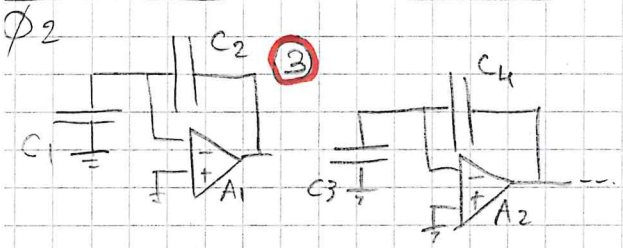
Non inverting integrator

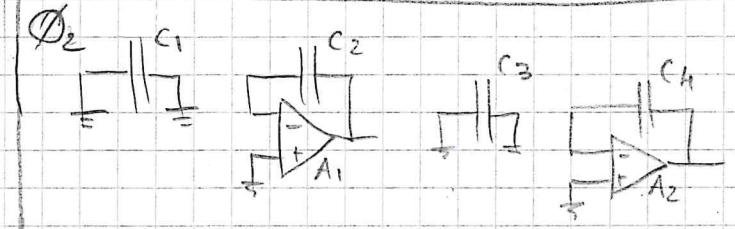


Inverting integrator









(1) V_{IN} charges C_1 in $T_{CK}/2$ (2) A_1 charges C_3 in $T_{CK}/2$

(3) A_1 settles to the updated V_{O1} value (but C_3 is disconnected so there is no load) in $T_{CK}/2$

(4) V_{IN} charges C_1, A_1 needs to consequently settle after V_{IN} change and at the same time load C_3 is attached. The same thing happens for every stage in the chain

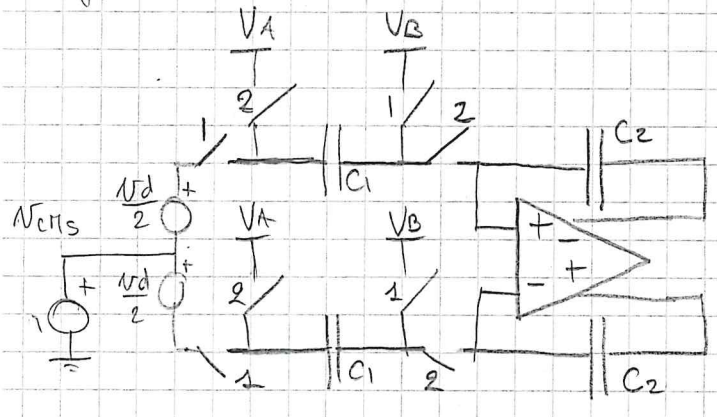
It's immediately clear that because of (4), A_1 and A_2 of the inverting configuration need to have a way larger BW of A_1, A_2 of the non-inv one. This is done because everything needs to be settled before $T_{CK}/2$.

We can conclude that, aside sign and pure delay, the non-inv configuration relaxes the settling time requirement a lot

(RINV = 9 ÷ 2 RINV)

62) Fully differential SW cap structure

We already mentioned that it's very difficult to implement single ended sw. cap filters:



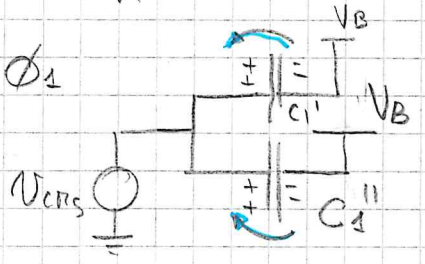
We already disscussed it:

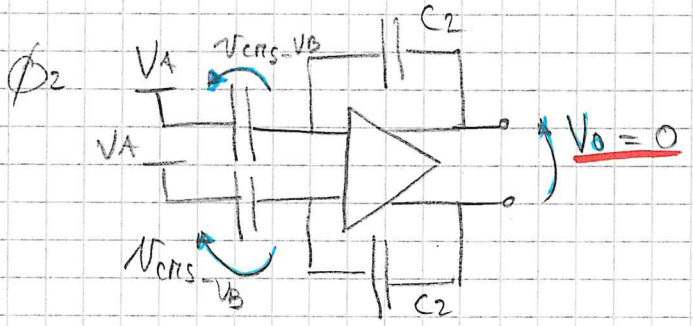
out V_{cm} → set by CMF only (if $Gloop_{CMF} \to \infty$)

in V_{cm} → set by V_{CMS}, V_A, V_B:

$$V_{CM_{IN}} = V_A + V_B - V_{CMS}$$

Why is it difficult to implement single ended sw filters? Mainly because of CM: with fully diff. structures what matters now is the difference between charges on C_1. For differential signals it is obvious, but look at CM:

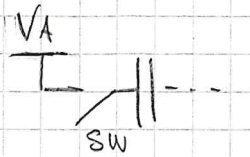




Φ_1: V_{CMS} is actively charging C_1', C_1'' by $V_{CM} - V_B$

Φ_2: charge on C_1', C_1'' is actually moving to V_{OUT}, but since it is the same quantity and ideal V_{OUT} senses differential charges only, the result is zero

Remember that sw.cap filters very often use sw.cap CMF switch structure



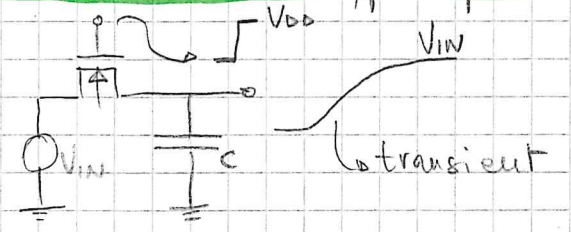
→ if $V_A \sim V_{DD}$ → pMOS sw is used

→ if $V_A \sim gnd$ → nMOS sw is used

→ if $V_A \sim V_{DD}/2$ → complementary pair must be used

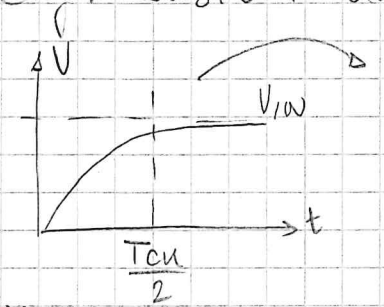
In general, we try to design V_A, V_B so that the SW is a single MOS because of the easier clock distribution to manage

63) The sw. type problem



SW selection and design is a complicated problem. We want to avoid glitches, artifacts, noise, settling time

e.g: consider an ideal RC response: $\tau = R_{ON\,sw} \cdot C$. V_{IN} is a step:



@ $\frac{T_{cn}}{2}$ we have a residual ΔV. Given the same τ, this ΔV risks being too much if the ADC has high resolution (e.g 20 bit)

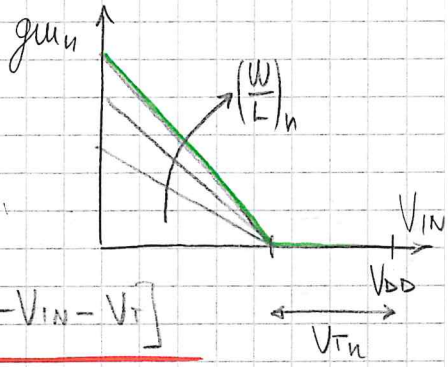
What can we do? → Reduce C so $\tau \downarrow$ → higher noise (kT/C)
→ Reduce R_{ON} so $\tau \downarrow$ → wider MOS → C_{gs}, C_{gd} ↑

In the second, we end up with larger occupied area and higher charge injection -

nMOS switch

$$I = \mu_n C_{ox}' \left(\frac{W}{L}\right)\left[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

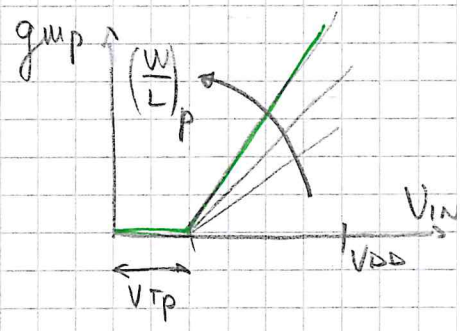
$$g_{on} = \frac{I}{V_{DS}} = \mu_n C_{ox}' \left(\frac{W}{L}\right)(V_{GS}-V_T) = \mu_n C_{ox}' \left(\frac{W}{L}\right)\left[V_{DD}-V_{IN}-V_T\right]$$



Note: g_{on} depends on V_{IN} → LTV response (not the usual RC).
It's better to work near 0V so g_{on} is high

pMOS switch

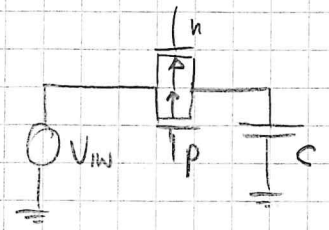
$$g_{op} = \mu_p C_{ox}' \left(\frac{W}{L}\right)_p \left[V_{IN} - |V_{Tp}|\right]$$

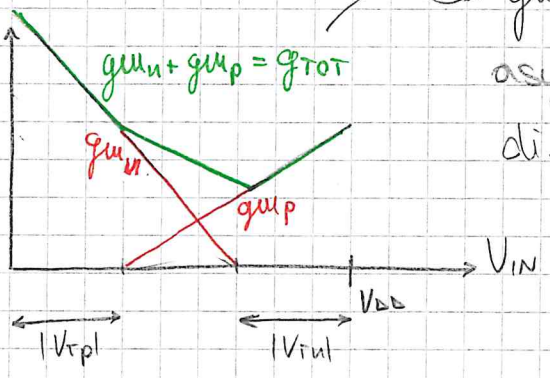


Exactly the same discussion made for nMOS.
Note that now, in order to have a high g_{on}
$V_{IN} \to V_{DD}$

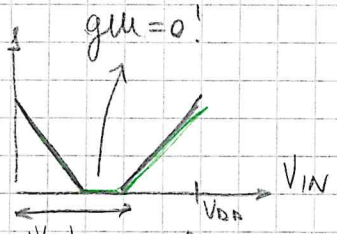
What if the signal swings from 0 to V_{DD}?

Transmission gate switch



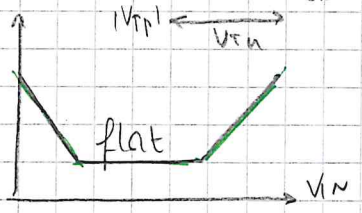


→ g_{mp}, g_{mn} slopes can be asymmetrical because of different μ, $\left(\frac{W}{L}\right)$, ...



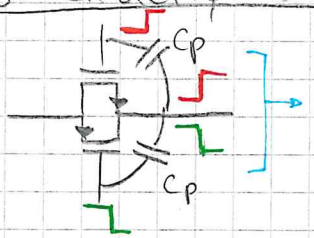
Note: $V_{Tn}+|V_{Tp}|<V_{DD}$ ⇝ but it's a tech problem →

Condition to have a flat $g_{m_{TOT}}$ in the middle is $\mu_n\left(\frac{W}{L}\right)_n = \mu_p\left(\frac{W}{L}\right)_p$ ①



This is preferred in HF samplers because of less LTV distortions (gm is flat in the middle → V_{IN} does not change its value)

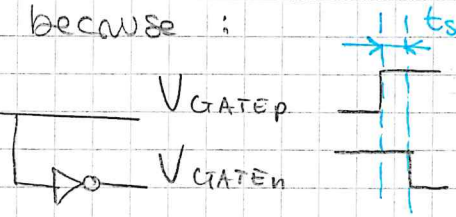
Generally $\left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_p$ ② is preferred because equal transistors areas means simpler, symmetrical layout and charge injection is exactly the same;



→ C_p are the same → balanced charges on V_c

Therefore, the choice between ① or ② depends on the application

Here in general, it's advisable not to use transmission gates at all because:



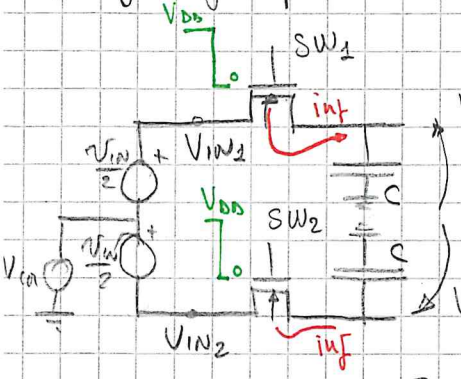
→ Logic used to generate the driving signals introduce skew. This means that nMOS and pMOS switch at different time instants.

Also, clock is affected by noise → aperture noise of the switch.

At HF we increase the dissipated power and have a more complex clock management to mitigate jitter → main source of power diss.

6.4.1 Charge injection compensation

By going fully differential, charge injection will be CM:



$V_{CM_{IN}} + \frac{V_{IN}}{2} + \frac{\Delta Q_1}{C_{par}}$

$V_{CM_{IN}} - \frac{V_{IN}}{2} + \frac{\Delta Q_2}{C_{par}}$

$V_{DIFF\,AMP}$ → Where Q is given by the following

$Q_{INJ} = (C_{ox} WL) \propto [V_{DD} - V_{IN} - V_{TH}]$ → V_{IN} depends on SW

If we look at SW_1 and SW_2 V_{IN} is different:

$V_{IN_1} = V_{IN} + \frac{V_{IN}}{2}$ $\quad V_{IN_2} = V_{IN} - \frac{V_{IN}}{2}$

This means that $\frac{\Delta Q_1}{C_p} \neq \frac{\Delta Q_2}{C_p}$

But, the difference is somewhat proportional wrt V_{IN} so it's not a big issue. Call this proportionality factor β → $\frac{\Delta Q}{C_p} = \pm \beta \frac{V_{IN}}{2}$

$V_{DIFF\,AMP} = V_{CM_{IN}} + \frac{V_{IN}}{2} + \beta \frac{V_{IN}}{2} - \left(V_{CM,IN} - \frac{V_{IN}}{2} - \beta \frac{V_{IN}}{2}\right) = V_{IN}(1+\beta)$

where β is small.

Since it's linear → no distortion

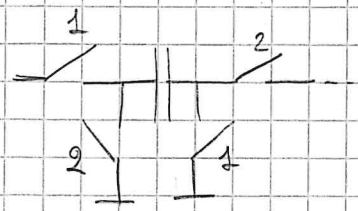
Body effect on charge injection

MOS threshold V_T depends on V_{IN} → critical for high performance converters

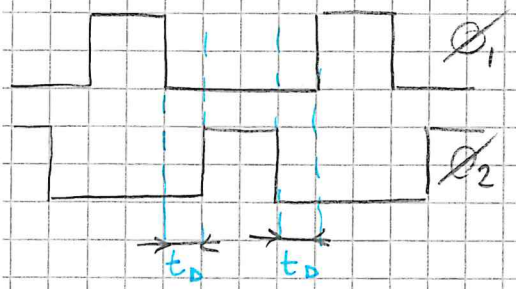
$Q_{INJ} = (C_{ox} WL)\left[V_{DD} - V_{IN} - V_{TH}\right]$ → $V_{TH} \cong V_{T0} + \gamma\left[\sqrt{V_{IN} + \phi} - V\phi\right]$

Because of the nonlinear relation → distortion

6.5) Dead time and Bottom-plate Sampling

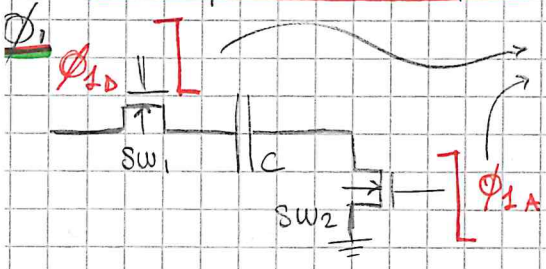


Because of the before-mentioned clock management issues we HAVE TO introduce some <u>dead time</u> between phases



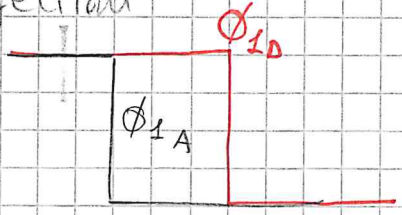
t_D must be large enough so that we mitigate all the tsettling, skew, RC response, ...

Bottom-plate Sampling to control charge injection



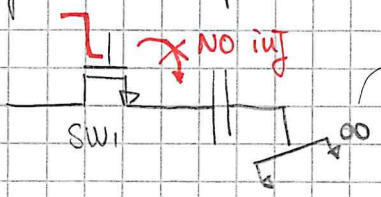
ϕ_{1D} = delayed ϕ_1

ϕ_{1A} = anticipated ϕ_1



We sample when sw_2 is open

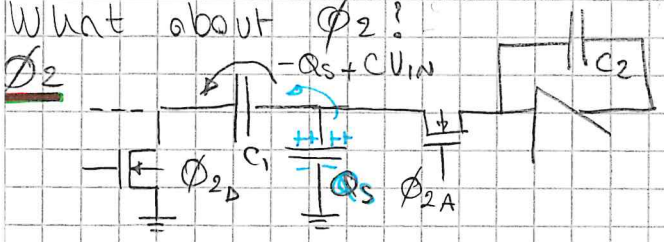
If sw_2 opens before sw_1, we can't ideally inject any charge:



We see ∞ resistance therefore no charge can be injected by sw_1

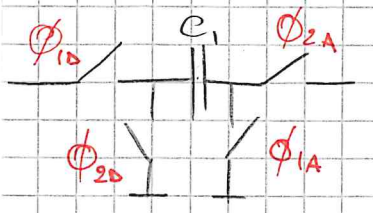
What about <u>sw_2 injected charge</u>? It's a CM contribution so <u>CMRR</u> will take care of that. We therefore need 4 total clocks. Note that a transmission gate sw filter stage needs 8 clock signals (ϕ_{1An}, ϕ_{1Ap}, ϕ_{2An}, ϕ_{2Ap}, ϕ_{1Dn}, ϕ_{1Dp}, ϕ_{2Dn}, ϕ_{2Dp})

What about ϕ_2?



ϕ_{1A}: Q_S flows to C_2

ϕ_{1D}: $-Q_S+CV_{IN}$ flows to C_2 so $Q_S-Q_S+CV_{IN}=CV_{IN}$ charge is balanced

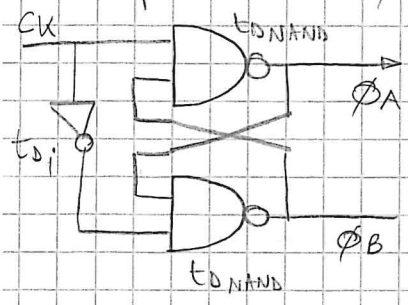


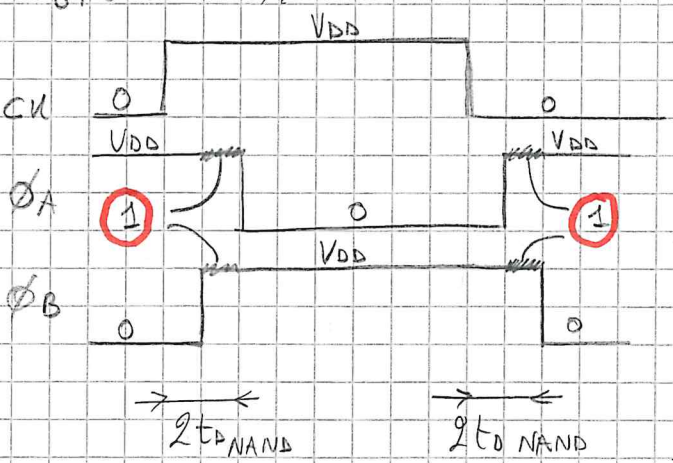
↳ This is the final 4 clocks and the relative switching orders. Keep in mind that since we can't control charge injection, Bottom-plate sampling is mandatory

6.5) Disoverlap phase generator

We need a circuit to generate the anticipated + delayed signals + dead time for the switches.

We assume the clock to be square (absolutely not true because @ 10Hz the 3rd harmonic at 30GHz would be well filtered by parasitics - - -).

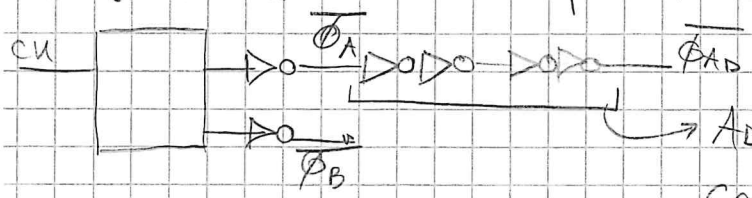




Suppose $t_{D\,INV} \ll t_{D\,NAND}$

We can drive a pMOS → when $\phi_A = \phi_B = V_{DD}$ (1), pMOS is off

To drive a nMOS we put inverters:

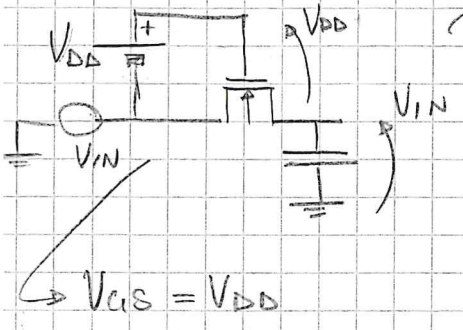


→ Additional delays for bottom plate sampling

Consider that the distribution of clocks is critical and it needs to cover a very large area → large power dissipation just for the clock busses (it's the most critical line in SW-cap circuits)

66) SW bootstrap

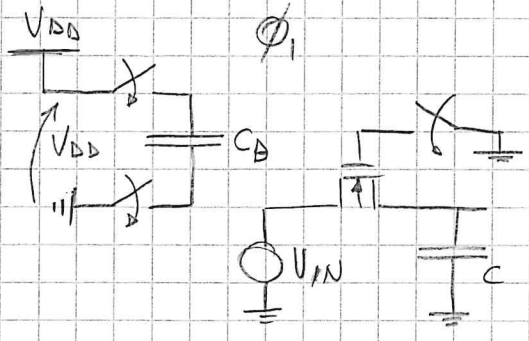
We use nMOS because of the smaller area (wrt pMOS).

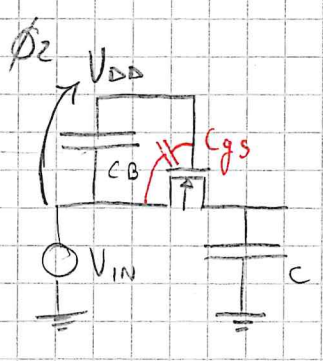


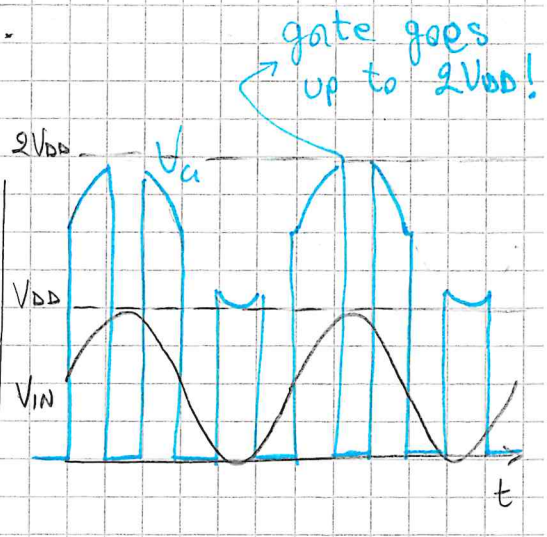
↳ By placing a battery between V_{IN} and the gate, we can exploit the full $0 \div V_{DD}$ range without the need for a transmission gate.

$\rightarrow V_{GS} = V_{DD}$

We can use a capacitor:

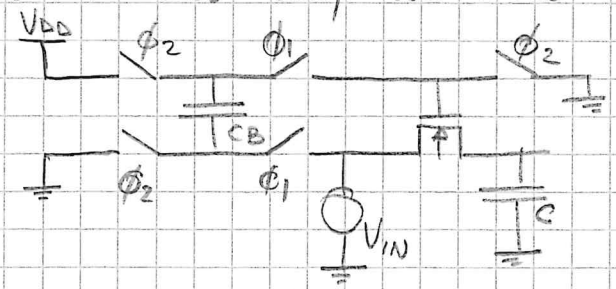






Note: in ϕ_2, $C_B \,//\, C_{gs}$ → because of charge sharing, the $V_{CB\,\phi_1} = V_{DD}$ will give a lower V_{GS} in ϕ_2 → C_B must be large enough so that the // does not lower V_{GS} too much.

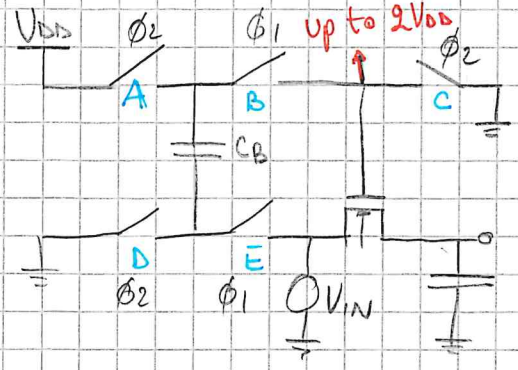
This is also why we need to restore C_B voltage in ϕ_1



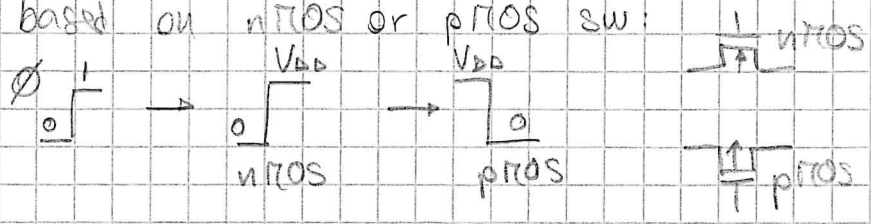
↳ SW design for bootstrap is critical because some of the SW need to be compatible with $\sim 2V_{DD}$ swings on their terminals. For this purpose, we could use TOS SW with thicker oxide layers, but they are usually slower and thus definitely useless for a high speed sampler.

Therefore we need 10/15 SW for driving just a single transistor using bootstrap!

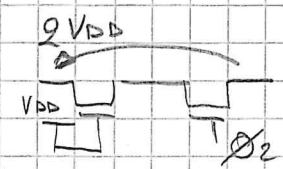
(67) Bootstrap implementation



Note that Φ_1, Φ_2 steps change based on nMOS or pMOS sw:

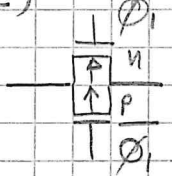


C, D switches are easy because they discharge to gnd → nMOS
They also have the same Φ_2 driving signal.



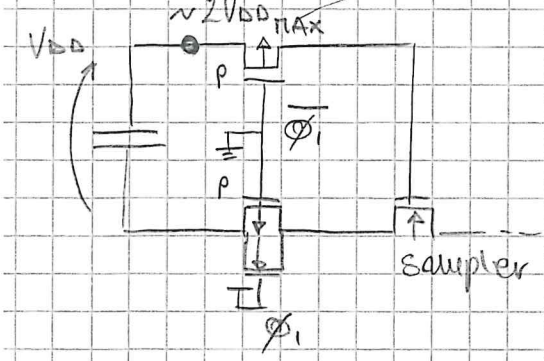
Note: even though there is a single switch they can be implemented with multiple MOS in order to distribute the $2V_{DD}$ as V_{DS} (look at sw C)

E swings from 0 to V_{DD}: transmission gate →

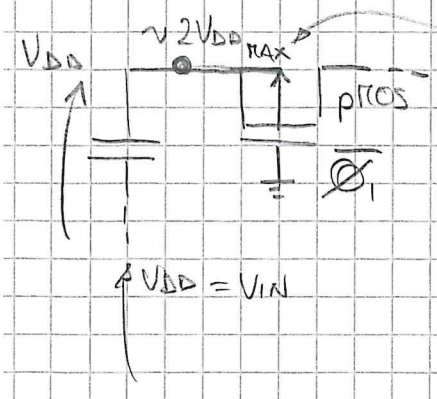


B, together with A, is the most critical because it/they can swing up to $V_{SIG} + V_{DD} \sim 2V_{DD}$.

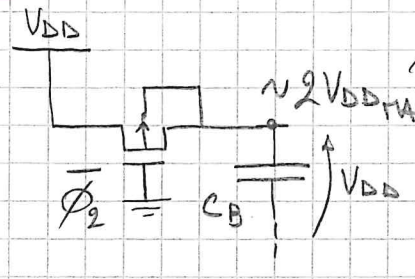
During on phase:



Be careful, since this point can go up to $2V_{DD}$, if we connect the body to just V_{DD} it won't be the highest positive voltage in the circuit. For this reason, for this particular pMOS, we connect the body to C_B instead of the typical V_{DD}:

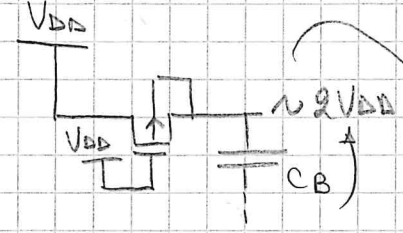


- A switch:



→ Pay close attention to the body diode connection! Now the most positive voltage node is at the right (unlike sw B).

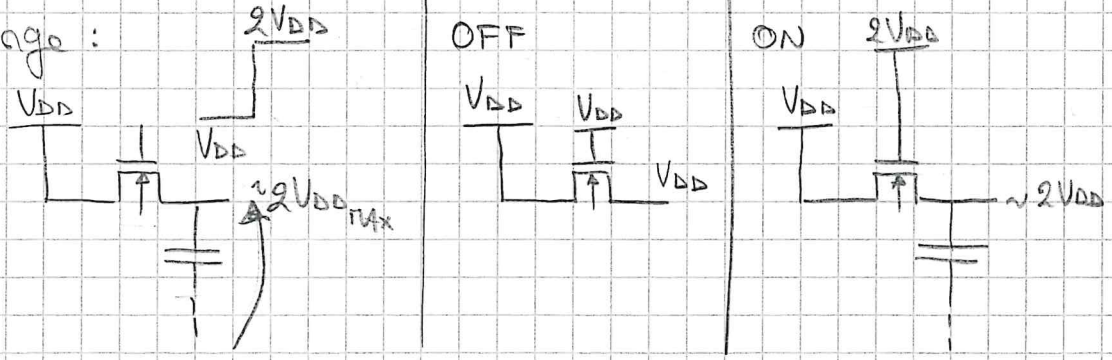
However we have a problem: during off operation it should be off, right?



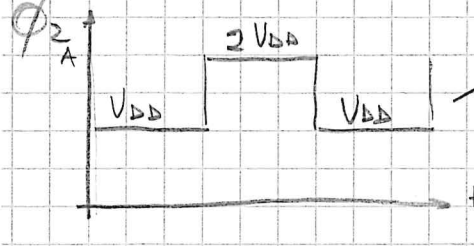
→ It's obviously on →

↗ Kind of like this transdiode

This means that we're discharging the C_B capacitor to V_{DD}. Solution, we implement a transistor with larger voltage:



The issue is now to generate a $\phi_2 + V_{DD}$ signal:

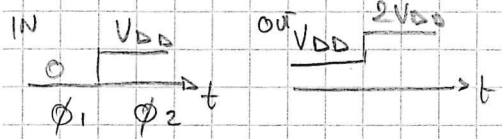


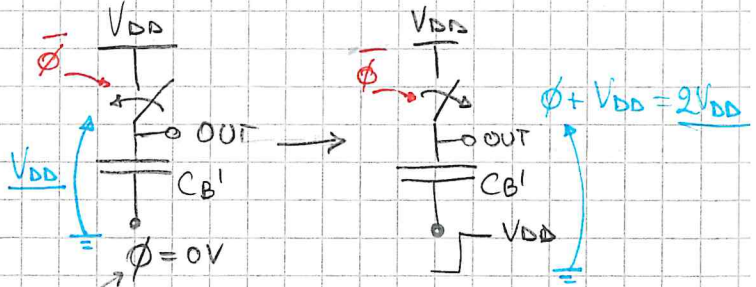
→ $\phi_2 + V_{DD}$

→ We can use the Nakagome charge pump

68) Nakagome charge pump

Goal: shift ϕ by V_{DD}:

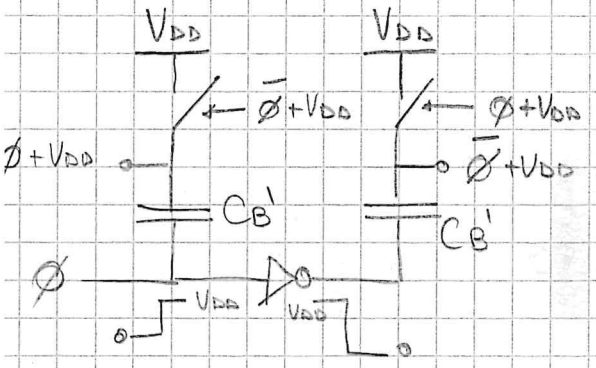


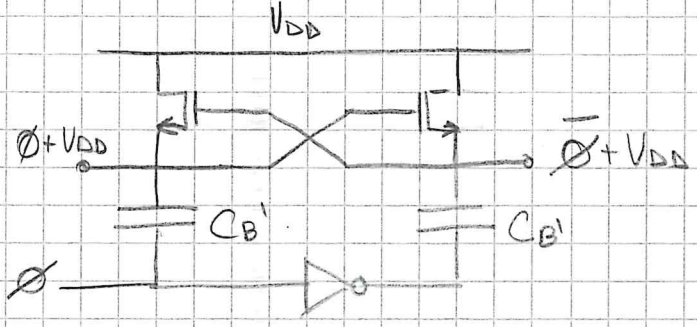


ϕ_1: input signal ϕ is shorted to gnd, sw is closed by $\bar{\phi}$ and C_B' is charged to V_{DD}

ϕ_2: input steps to V_{DD}, sw is opened by $\bar{\phi}$ and V_{OUT} can now shift to $2V_{DD}$.

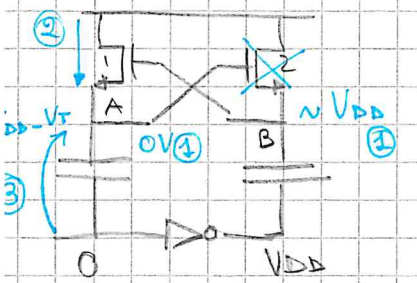
But, we have the same problem as before because $\bar{\phi}$ needs to be shifted by V_{DD} in order to work correctly. What can we do? Double the circuit:





How does it work? Consider the startup:

Step 0)



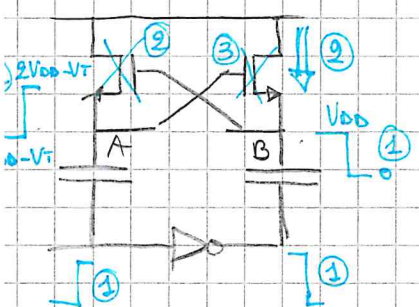
Initial condition: $\phi = 0$, $V_{C_B'} = 0$

① $V_{CB} = 0 \rightarrow A = 0V$, $B = V_{DD}$

② Since $B = V_{DD}$, Π_1 is on and some current flows, charging C_B

③ $V_{C_B'}$ goes up to $V_{DD} - V_T$

Step 1)



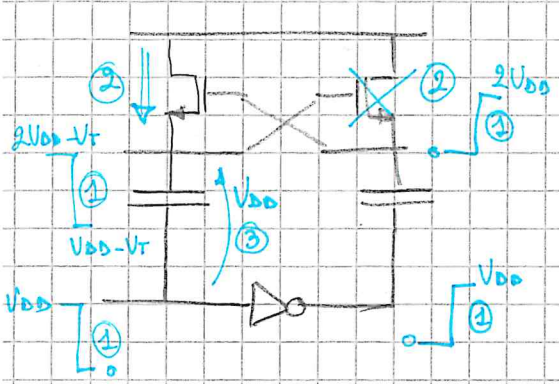
① ϕ jumps to V_{DD}, inversion on the right Capacitor C_B' shifts the voltage accordingly

② Since $B \rightarrow 0$, then Π_1 shuts off

Since $A \rightarrow 2V_{DD} - V_T$ then Π_2 is ON and it charges the right capacitor to V_{DD}

③ $A \rightarrow 2V_{DD} - V_T$, $B \rightarrow V_{DD}$ $\rightarrow$ both Π_1, Π_2 are now off because V_{GS} is neither sufficiently high for turning them ON

Step 3)

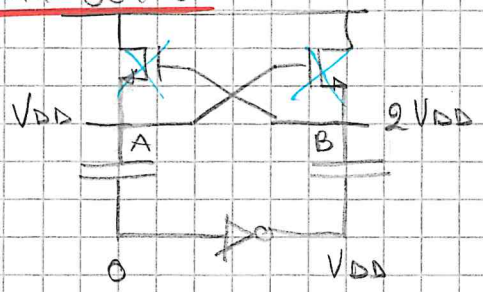


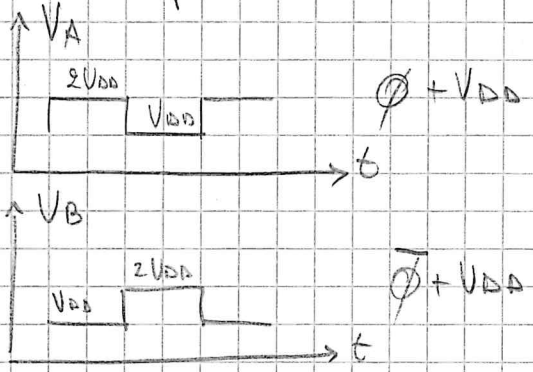
① ϕ shifts to 0 so $\bar{\phi}$, A, B shift down and up accordingly

② B → $2V_{DD}$, A → $V_{DD}-V_T$ so Π_1 is on and Π_2 is off

③ Π_1 charges C_B' to V_{DD} reaching the final state:

Final state

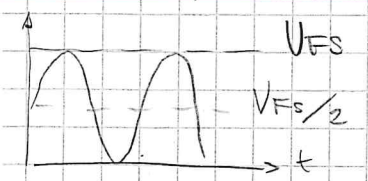




From now on, the process repeats itself.

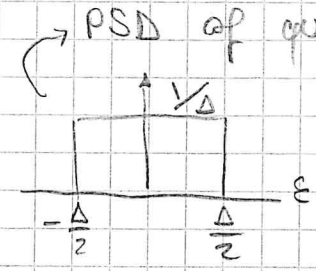
As we can see, considering all switches and this CP used for $\phi + V_{DD}$, we end up counting up to 15 TCKs just for driving a samples SW with a bootstrap.

69) Sampled noise, SNR, aperture noise



$\Delta = LSB = V_{FS}/2^B$

Quant. noise $\sigma^2 = \frac{\Delta^2}{12}$



$$SNR^2 = \frac{\left(\frac{V_{FS}}{2}\right)^2 \cdot \frac{1}{2}}{\left(\frac{V_{FS}}{2^B}\right)^2 \cdot \frac{1}{12}} = \frac{12}{4 \cdot 2} \cdot 2^{2B} = 1{,}5 \cdot 2^{2B}$$

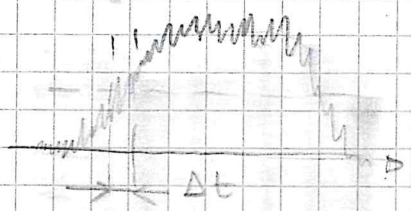
V_{IN} is taken at the best case → $V_{IN} = V_{FS}/2$ ← sine amplitude

$$SNR|_{dB} = 10 \log_{10}\left(\frac{3}{2}\right) + 10 \log_{10}\left(2^{2B}\right) = 1{,}76 + 6{,}02 \cdot B \rightarrow \text{rearrange} \rightarrow$$

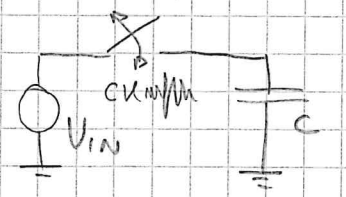
$$ENOB = \frac{SNR_{dB} - 1{,}76}{6{,}02} \sim \text{equivalent number of bits}$$

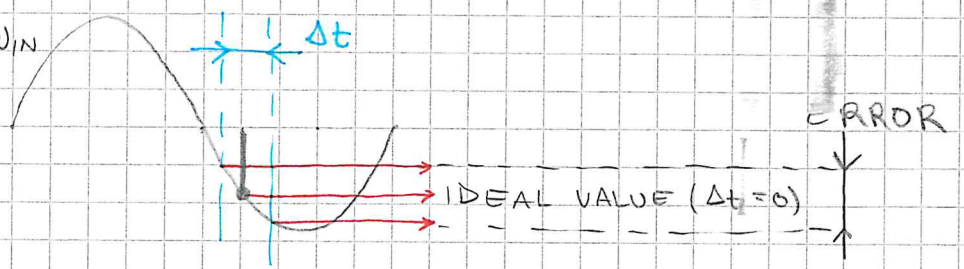
Usually, SNR is given and we compute the bits needed to achieve that SNR (e.g.: $SNR^2 = (A^2/2)/(kT/C)$)

Aperture/Jitter noise: CK is a noisy signal →



When we switch we get an uncertain time Δt given by jitter. To reduce it we must burn more power for the clock bus. Which are the consequences?

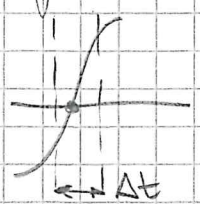




We commit an error during Δt, we think we're sampling right on the precise time instant but instead we get another value.

In which point do we commit the largest error?

Largest error is achieved at zero crossing because we have the largest slope



$V_{IN} = A_0 \cos(\omega_{IN} t)$ $\left.\frac{\partial V_{IN}}{\partial t}\right|_{MAX} = A_0 \omega_{IN}$ ⟶

$\Delta V_{MAX} = A_0 \omega_{IN} \Delta t$

The find variance will be $\overline{\sigma_{V_{MAX}}^2} = A_0^2 \omega_{IN}^2 \overline{\sigma_{\Delta t}^2}$

Therefore, at worst case we get:

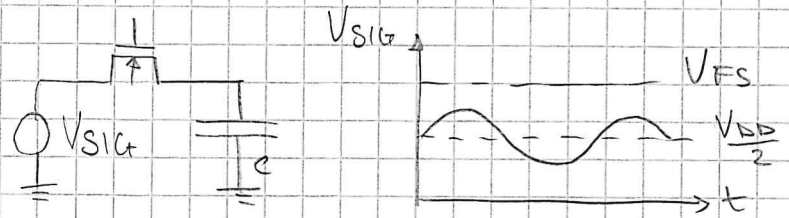
$$SNR\Big|_{Jitter}^2 = \frac{A_0^2/2}{\frac{A_0^2 \omega_{IN}}{2} \overline{\sigma_{\Delta t}^2}} = \frac{1}{\omega_{IN}^2 \overline{\sigma_{\Delta t}^2}} \Rightarrow SNR\Big|_{Jitter}^{dB} = 20 \log\left(\frac{1}{2\pi f_{IN} \Delta t}\right)$$

As f_{IN} ↗ it becomes more difficult to keep jitter down

e.g: $f_{IN} = 1\,GHz$ ($f_{CLK} > 2\,GHz$), $\sigma_{\Delta t} = 10^{-12}\,s$

$SNRdB\Big|_{Jitter} \cong 44\,dB \longrightarrow ENOB = \frac{44 - 1,76}{6,02} \cong 7\,bit$

70) Time Variant nonlinearity of the sampler

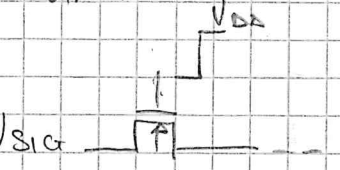


$V_{SIG} = \frac{V_{DD}}{2} + A \sin(\omega_{IN} t)$ where $A < \frac{V_{DD}}{2}$ we don't want hard clipping

Since the sampler must swiftly follow the input signal we say that $\omega_{IN} \ll 1/R_{ON} C$ (Keep in mind that we also need to satisfy Nyquist frequency)

Issue: no bootstrap → g_m changes with V_{IN}:

$$R \cong \frac{1}{\mu C_{ox} \left(\frac{W}{L}\right) [V_{GS} - V_T(V_{GS})]}$$ → Also $V_T \propto V_{GS}$



Where $V_{GS} = V_{DD} - V_{SIG} = V_{DD} - \frac{V_{DD}}{2} - A\sin(\omega_{IN} t) = \frac{V_{DD}}{2} - A\sin(\omega_{IN} t$

Keep V_T = constant, we won't discuss V_{GS} dependance

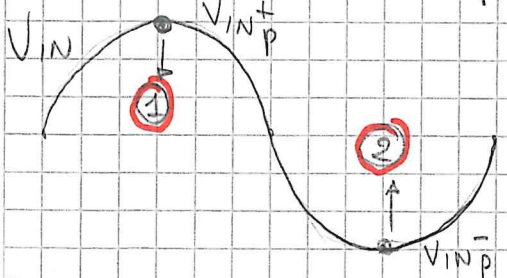
We used to say $\frac{V_O(s)}{V_{IN}(s)} = \frac{1}{1 + s RC}$ for a LTI system

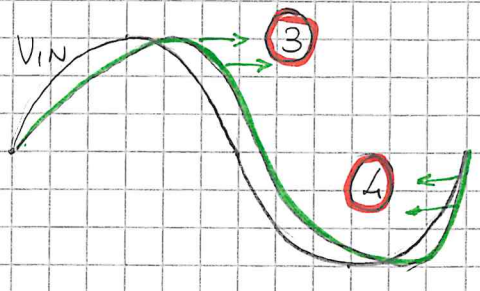
Laplace here does not help:

$I = C \frac{dV_{OUT}}{dt}$ $V_{SIG} = IR + V_{OUT} = RC \frac{dV_{OUT}}{dt} + V_{OUT}$

R also depends on V_{OUT} → Nonlinear differential equation

Let us see what happens





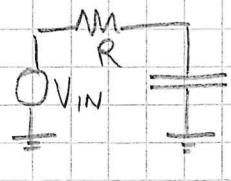
1) At V_{IN} positive peak, R increases → f_{pole} shifts at low f.
2) At V_{IN} negative peak, R decreases → f_{pole} shifts at high f.

We can see that the f_{pole} modulation phase shifts V_{IN}:

3) because of 1 we get an increased phase delay
4) because of 2 the phase delay decreases until it reaches the input and from there the waveform restarts

If we consider a small voltage drop on R → $V_{OUT} \cong V_{IN}$

We can then compute the magnitude of the current:



$$|I| = C A \omega_{IN} \cos(\omega_{IN} t) \quad (2)$$

We then Taylor-expand R value:

$V_{IN} = \frac{V_{DD}}{2}$ → bias

$$R \cong \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)\left[\frac{V_{DD}}{2} - v_{IN}(t) - V_T(v_{IN})\right]} = R_0 + r_1 v_{IN} + r_2 v_{IN}^2 \quad (1)$$

(V_{GS})

$R_0 \to [\Omega]$ $\quad r_1 \to \left[\frac{\Omega}{V}\right]$ $\quad r_2 \to \left[\frac{\Omega}{V^2}\right]$

When v_{IN} ↗ → R ↗ so r_1 ↗ and r_2 should increase as well

We now consider V_R not negligible anymore and we compute

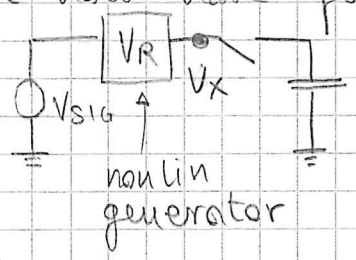
$V_R = R \cdot I = (1) \cdot (2) =$ Cosine · cosine multiplications - - - =

$$\cong R_0 C A \omega_{IN} \cos(\omega_{IN} t) + \frac{CA}{2} r_1 \omega_{IN} \sin(2\omega_{IN} t) - \frac{CA^3}{4} r_2 \omega_{IN} \cos(3\omega_{IN} t) + o.t.$$

o.t. = other terms)

We neglected minor double products. This is an already simplified discussion, we want to just give a hint on what's happening.

We now have fundamental, 2nd harmonic + 3rd harmonic.



We now analyze the spectrum on V_x

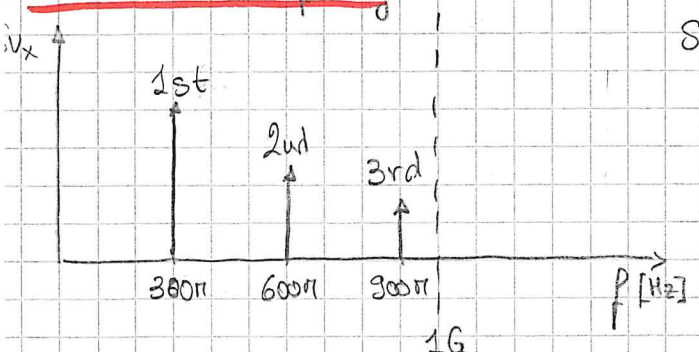
Considering also the effect of the switch

$$V_x = V_{SIG} - V_x = \frac{V_{DD}}{2} + A\sin(\omega_{IN} t) - R_0 C A \omega_{IN} \cos(\omega_{IN} t) + 2nd/3rd \text{ harmonics}$$

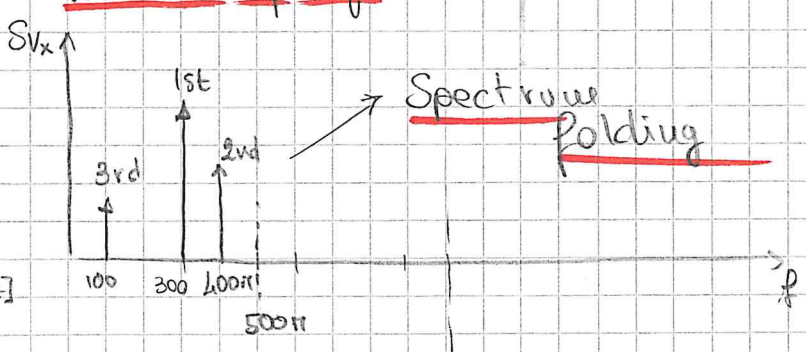
↳ $A \gg R_0 C A \omega_{IN}$ because we said $\omega_{IN} \ll \frac{1}{R_0 C}$ so $R_0 C \omega_{IN} \ll 1$)

$$V_x \cong V_{DD}/2 + A\sin(\omega_{IN} t) + \frac{CA}{2} r_1 \omega_{IN} \sin(2\omega_{IN} t) - \frac{CA^3}{4} r_2 \omega_{IN} \cos(3\omega_{IN} t)$$

Without sampling



With sampling



Let us now quantify the distortion

$$HD_2 = \frac{C\frac{A^2}{2}\omega_{IN} r_1}{A} \qquad HD_3 = \frac{C\frac{A^3}{4}\omega_{IN} r_2}{A} \qquad HD_{TOT} = \left|\sum_i |HD_i|\right|^2$$

THD

THD = Total Harmonic Distortion. It should be included in the SNR/ENOB computation.

Bootstrap will reduce this HD by a lot, but it won't cancel it. In fact, we did not take into account $V_T = f(V_{IN})$

We can't reduce reduce V_{IN} amplitude for a better SNR because noise does not decrease:

$$SNR = \frac{A^2/2}{\frac{kT}{C}}$$ → if we lower A by $\frac{1}{2}$, capacitance needs to be increased $\times 4$ to keep SNR the same

$$HD_2' = C'\frac{A'}{2}\omega_{IN} r_1 = 4C\cdot\frac{A}{2}\cdot\frac{1}{2}\omega_{IN} r_1 = 2HD_2$$

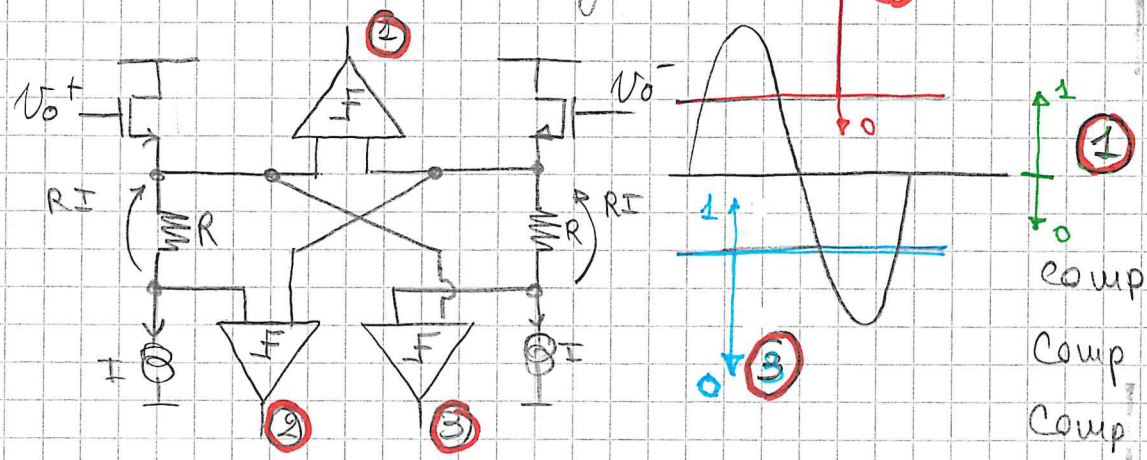
Distortion of the 2nd harmonic is doubled

$$HD_3' = C'A'^2\cdot\frac{1}{4}\omega_{IN} r_2 = 4C\cdot\frac{1}{4}A^2\frac{\omega_{IN} r_2}{4}$$ → HD_3 does not change

This is the proof why lowering V_{IN} amplitude is always a bad idea.

To) Insight on threshold voltage generation for comparators

Fully differential comparators do not have an available "threshold" input. How can we do that? Consider a flash converter resistor string.



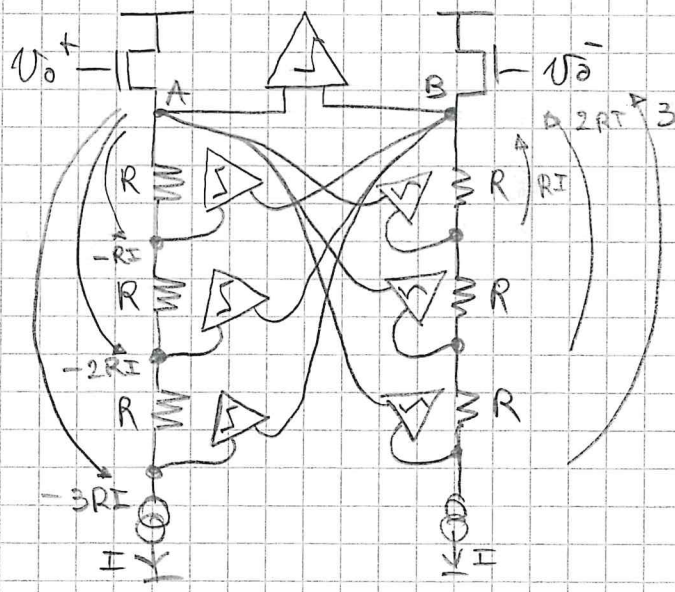
comp 1 : 0 ref

Comp 2 : RI ref

Comp 3 : -RI ref

We get a thermometric digital output

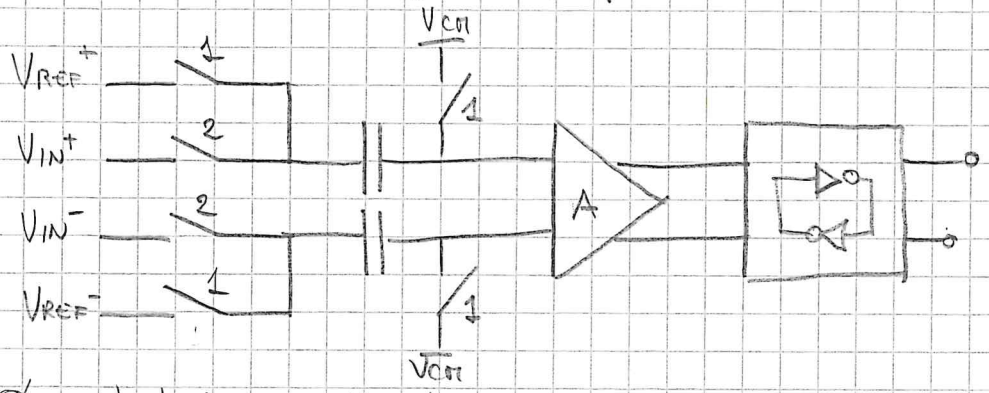
If we use a resistor strip:



Comparators take A, B points for one input and then RI, 2RI, 3RI, -RI, -2RI, -3RI → other comp input

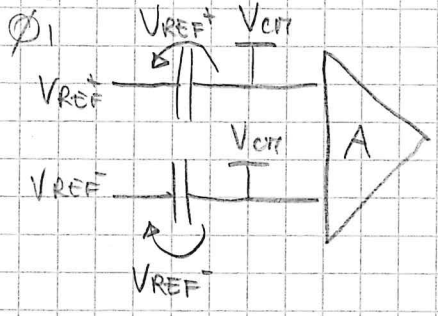
SW capacitor comparator threshold

Note: the following configuration does not sample the offset.

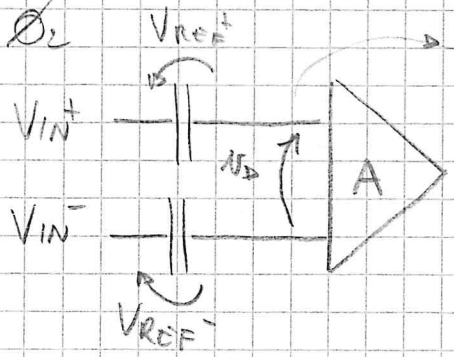


ϕ_1: latch reset phase.

Suppose $V_{CM} = 0$



↝ capacitors are shorted to the CM of the preamp and store V_{REF}



$\rightarrow V_D = (V_{IN}^+ - V_{IN}^-) - (V_{REF}^+ - V_{REF}^-)$

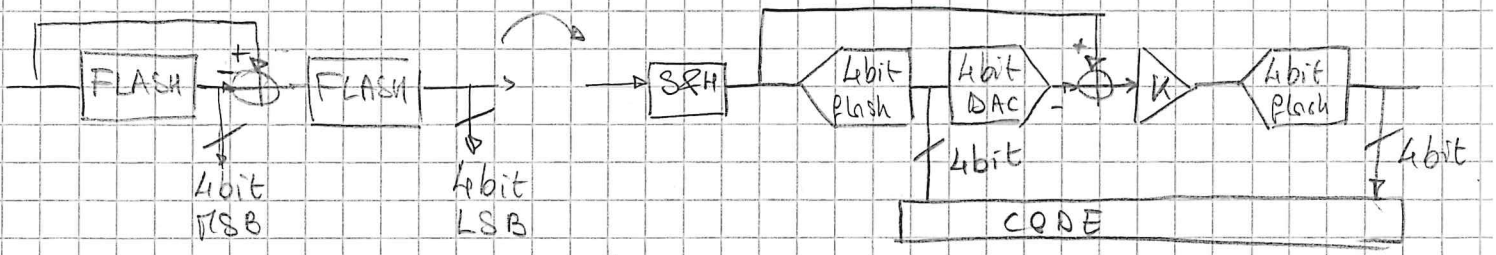
We got a fully differential threshold

There is no best threshold generation, it depends on the application.

For example, since this does not perform CDS, it can't be used in interleaved/pipelined converters in which offset is critical.

11) Pipelined ADCs

※ comparators can be huge for some architectures (e.g. 256 comp for 8 bit flash). We can do a split:



1st flash = coarse converter 2nd flash = fine converter

$K = 1$ or 2^m in our case $m = 4$ so that we exploit the full scale range for the residue in the fine converter

residue ~ amplitude ↗ $\frac{V_{FS}}{4}$ — K — RESIDUE ~ amplitude ↗ V_{FS} — flash

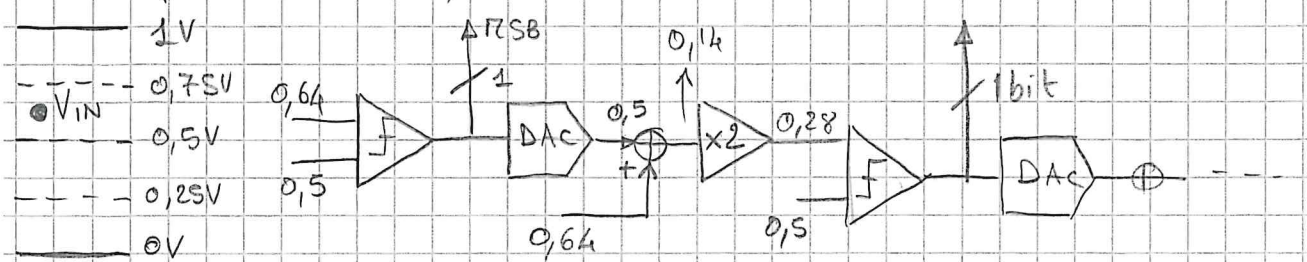
If we pipelined the structure, we could run at full speed. However, settling and BW of the opamps will limit the speed.

e.g.:

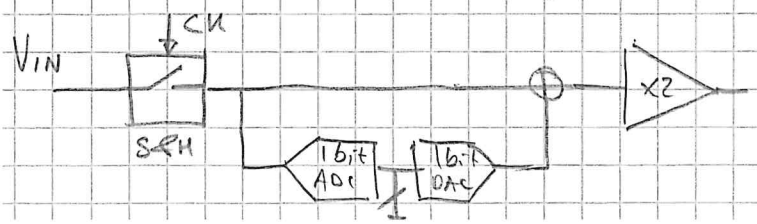
- $K = 2^m$ we amplify → BW of the gain stage is lower thus BW of the full ADC is lower but thresholds of the 1st and 2nd flash are the same
- $K = 1$ higher BW but we need to generate more thresholds

Typically, high speed is achieved with 1 bit stages ($K = 2$)

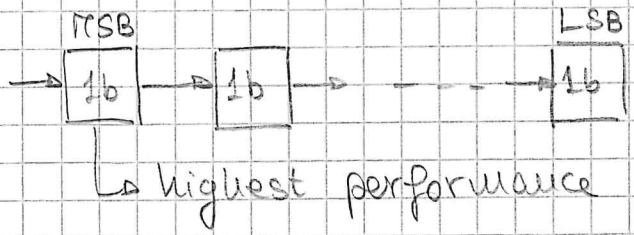
example: $V_{IN} = 0,64V$



With a repeated stage we end up with



Keep in mind that MSBs are the most critical stages in terms of noise/linearity/etc because they are the most important! It wouldn't make sense to have the same requirements of the MSB stage on the LSB one.



↳ highest performance

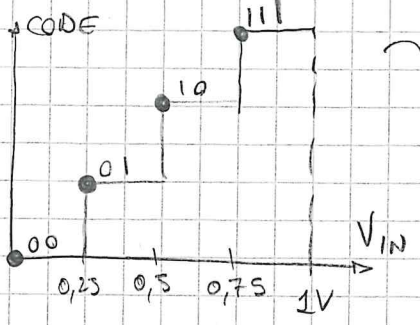
↝ least critical wrt offset / noise / linearity ...

This way, we can relax the power dissipation and matching requirements on the following stages.

These pipelined 1 bit flash are typically used in 10/12/16 bit and 10 MHz ÷ 100s of MHz converters

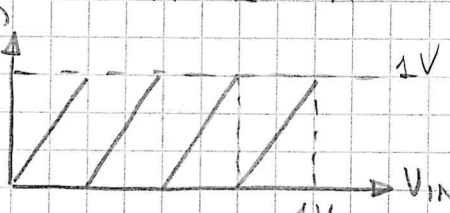
12) Residual voltage and glitches/errors

Let us now focus on the 1st stage structure. 2 bits ADC:



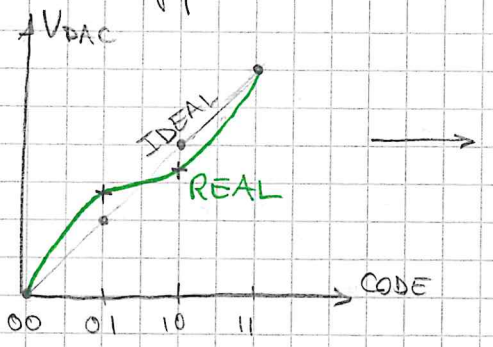
↳ Black points should be translated to the center of the step not to have offset but we don't care, it's just for visualization. $K = 2^2 = 4$:

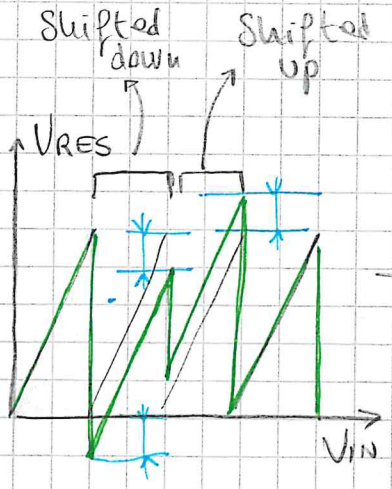
$$V_{RES\ stage}^{1st} = 2^2 \left[V_{IN} - V_{DAC\ stage}^{1st} \right]$$

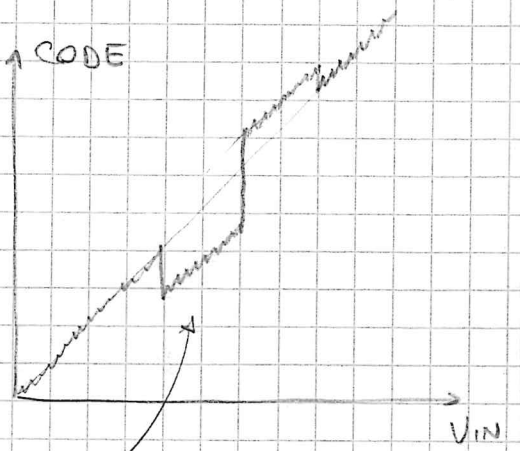


Nonlinearities in ADCs, DACs will influence the real static characteristic:

- DAC offset error:

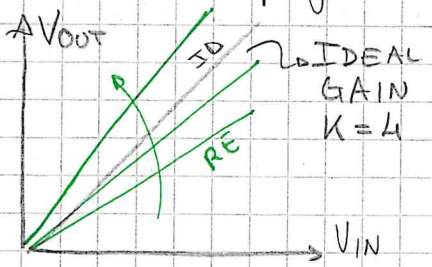


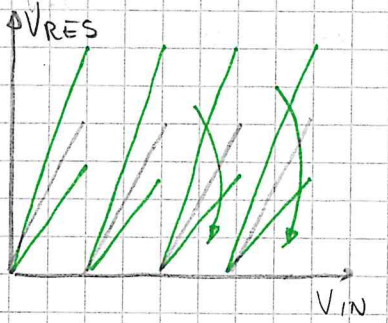


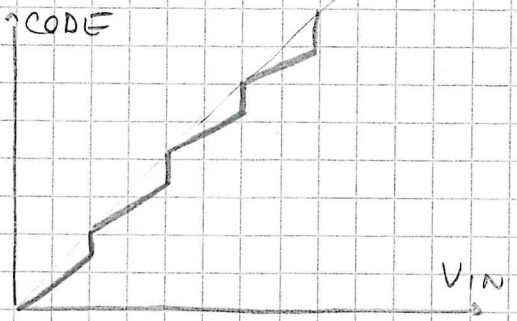


The static characteristic can show a shift

- Residual amp gain error







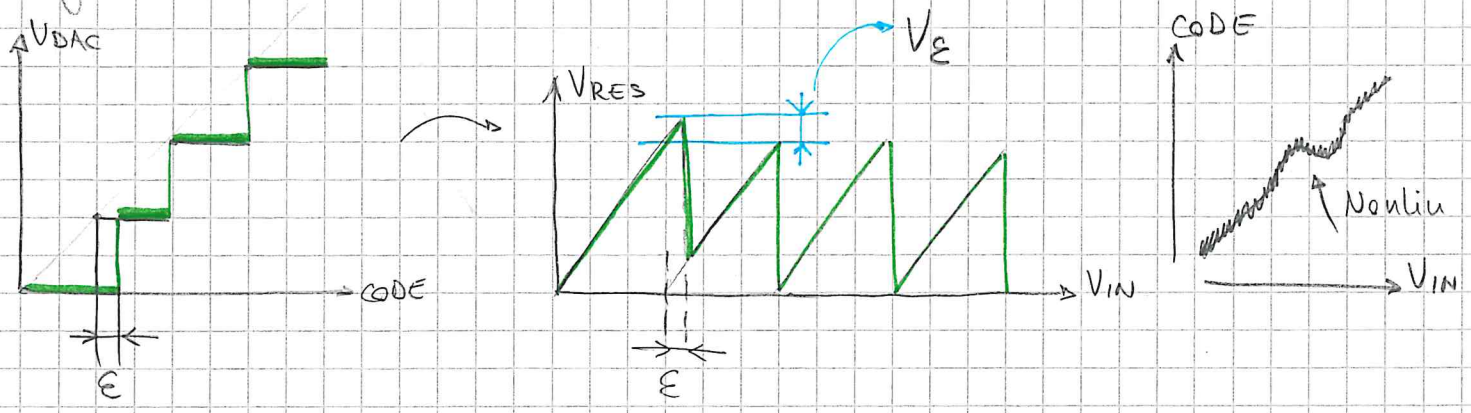
We said that gain error of the amp is a linear one, but here it becomes detrimental to the full structure.

Many other errors are difficult to discuss but they all contribute to a nonlinear static characteristic

We'll see in detail what happens if one of the ADC comparators is affected by offset and how to compensate it with the redundancy technique

73) Redundancy technique

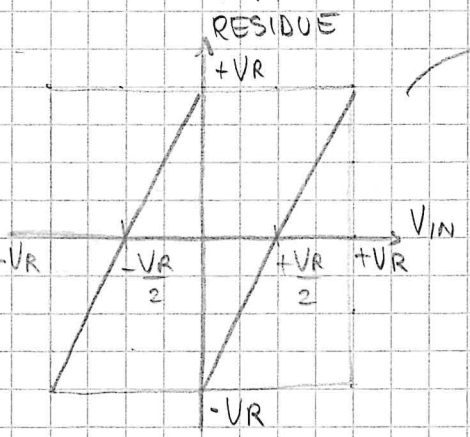
If one of the comparators is affected by an offset, we get a vertical error in $V_{RESIDUAL}$



$V_\varepsilon = \varepsilon \cdot 2^{m} = 4\varepsilon$ for a 2 bit pipelined stage

On the final characteristic we get a nonlinearity

In fully differential structures, $V_{RESIDUAL}$ will be:



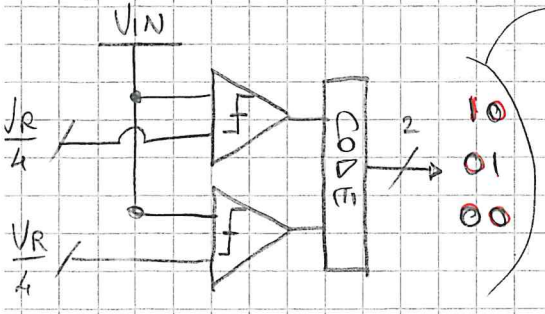
→ $\pm V_R$ is a direct consequence of the fully diff structure.

To remove the comparator offset we can apply the redundancy technique

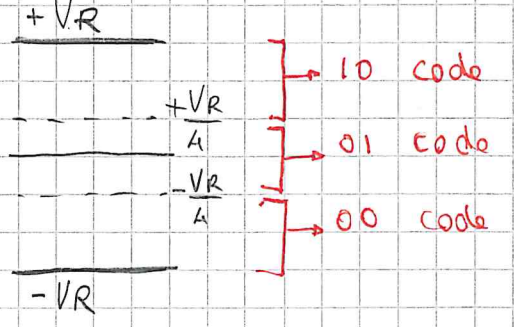
→ redundant

Idea: we do something extra that is in principle not needed but it's done to recuperate the offset error.

In the flash ADC, use two comparators instead of the usual single one:



Thresholds will be the following →

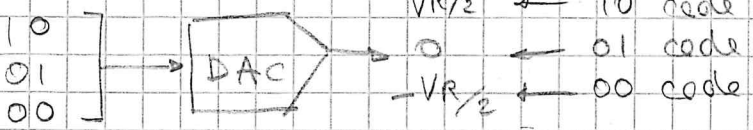


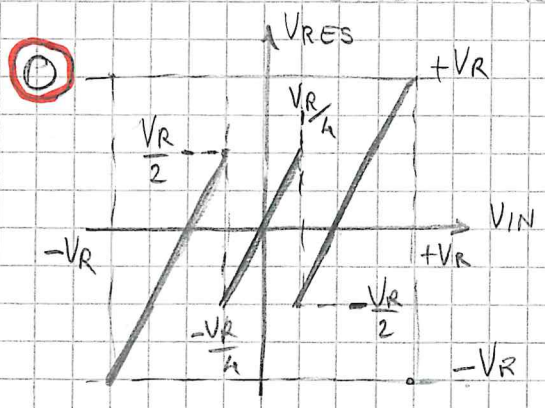
So: $+\frac{V_R}{4} < V_{IN} < +V_R$ → higher half → 10

$-\frac{V_R}{4} < V_{IN} < +\frac{V_R}{4}$ → middle → 01

$-V_R < V_{IN} < -\frac{V_R}{2}$ → lower half → 00

Therefore we moved from 1 bit ADC to ~2 bits. DAC now is 2 bits as well:

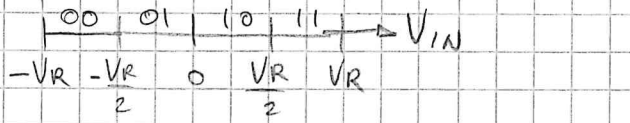




By subtracting V_{IN} and V_{DAC}:

Working principle

Consider a 2 stage pipelined ADC without any offset. that uses the redundancy technique. Total bits will be 2 and the code output will be:



① $-V_R < V_{IN} < -\frac{V_R}{2}$ → code 00 ② $-\frac{V_R}{2} < V_{IN} < 0$ → code 01

③ $0 < V_{IN} < \frac{V_R}{2}$ → code 10 ④ $\frac{V_R}{2} < V_{IN} < V_R$ → code 11

We will divide the analysis in 4 cases to cover all $-V_R$ to $+V_R$ range, but we will cover only some ranges because the negative part is symmetrical so discussion is the same:

- $V_{IN} > \frac{V_R}{2}$ → comparators output 10 and $V_{Residual}$ (plot ①) is of course >0.

  2nd stage, since it's the LSB, will be a simple comparator that distinguishes $\gtrless 0$ only. Since $V_{RES} > 0$ → LSB = 1

  We now perform an addition considering the 2 bit 1st stage and 1 bit second stage (LSB)

  1 0 → 1st
  1 → 2nd
  1 1 ——→ Result is consistent with ④

- $V_{IN} < -V_R/2$ → comparators of the 1st stage output 00 and $V_{RESIDUAL} < 0$ so LSB out = 0

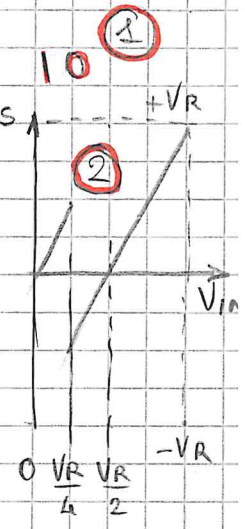
  0 0 ← 1st
  0 ← 2nd
  0 0 ——→ Result is consistent with ①

We covered the obvious cases

Let us now see the range $0 < V_{IN} < \frac{V_R}{2}$. In the VRESIDUAL we will see either 10 or 01 (unknown). The redundancy technique, when an unknown 01 is generated, treats it like a carry bit that will be propagated in the sum:

Recall that for $0 < V_{IN} < \frac{V_R}{2}$ → pipelined ADC code is 10

$\frac{V_R}{4} < V_{IN} < \frac{V_R}{2}$ Comparators of the 1st stage generate a 10. We can now see that the residual voltage (plot ②) is <0 so LSB out will be 0:

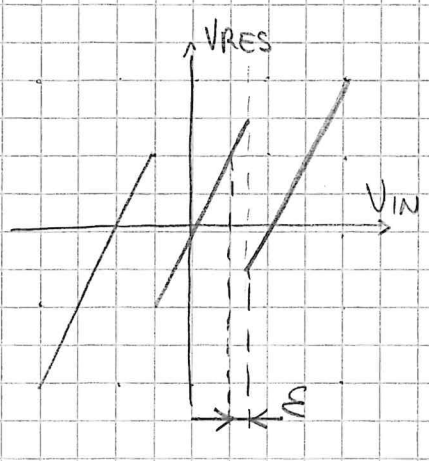


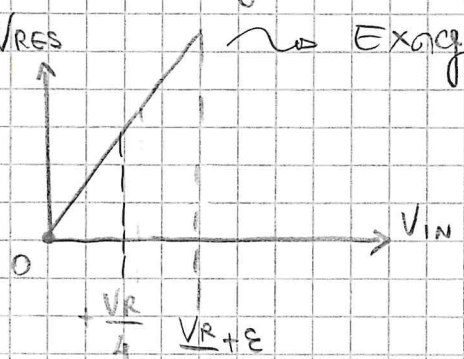

```
 1 0  ← 1st
   0  ← 2nd
 1 0  → Result is consistent with 1
```

$0 < V_{IN} < \frac{V_R}{4}$ comparators generate a 01 because it's in the unknown range. We can see that $V_{RESIDUAL}$ is >0 (plot ②) so LSB out will be 1:

```
 0 1  ← 1st ↝ kind of a carry bit propagated to next stage
   1  ← 2nd
 1 0  → Result is consistent with 1
```

We verified that for every input voltage, the pipelined ADC output does not change. Ok great, we did twice the work but for what? Suppose now that the comparator has an offset. This system will still generate the correct code:





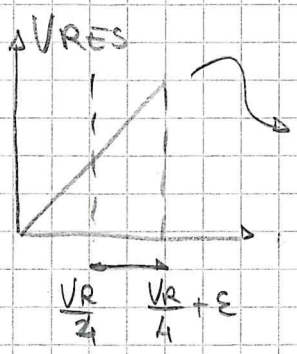
↝ Exaggerated view of ε

We can now see that the 01/10 separation moved:

01 | 10 → 01/10 separation with offset

01 | 10 ↝ 01/10 separation w/o offset (previous)

- $\frac{V_R}{4} < V_{IN} < \frac{V_R}{4} + \varepsilon$ ⇝ without offset, this would have been in the 10 output region, but now it gives 01

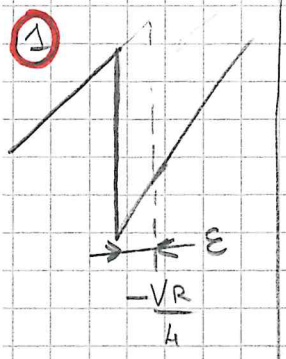


But now $V_{RESIDUAL}$ is >0 therefore LSB is 1

01 ← 1st
1 ← 2nd
10 → Result is consistent with the output without offset

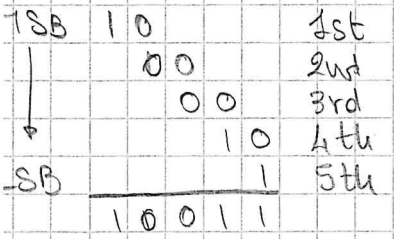
The same exact thing happens with $V_{IN} < 0$ and ε restricts the 01 zone ($V_{RESIDUAL}$ plot would then be (1))

(1)

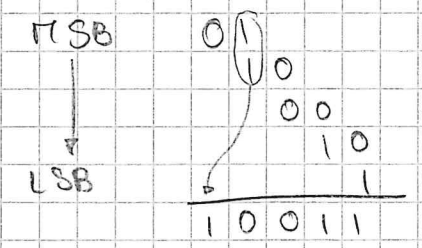


What happens if offset is affecting the comp of the LSB? I must devise something else since it is the last bit and there is no following stage to propagate the carry bit to.

More in general, for multiple stage pipelines, the situation will be (e.g with 5 stages)



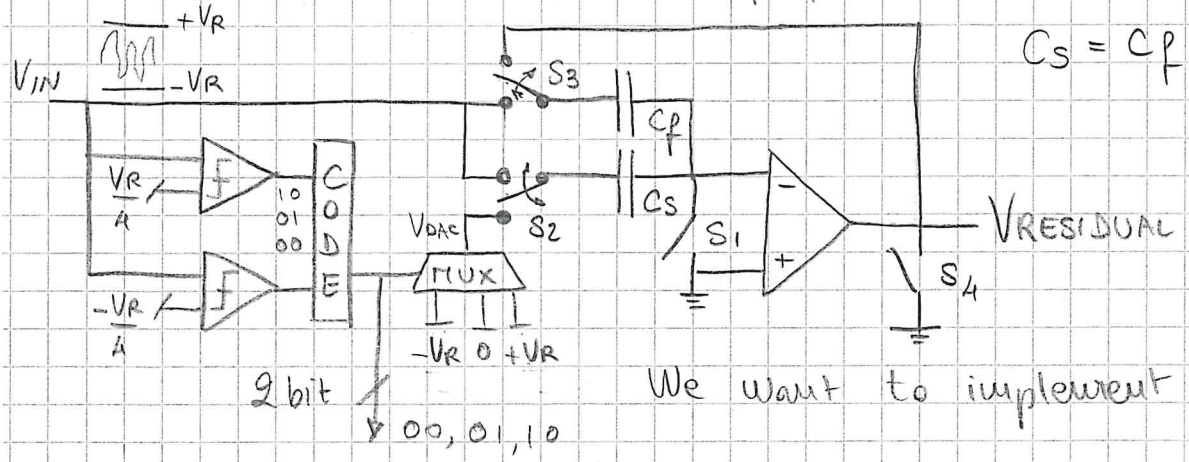
Case where there is clear decision



Case where there are unknown values (same input V_{IN} but the pipelined ADC has offsets)

7-4) Redundancy technique circuit description

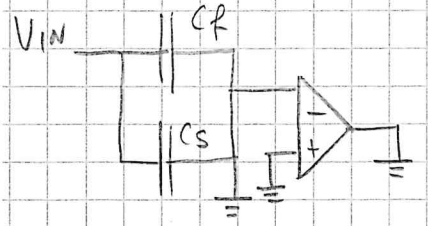
S&H is embedded into the amplifier and we need $K = 2$



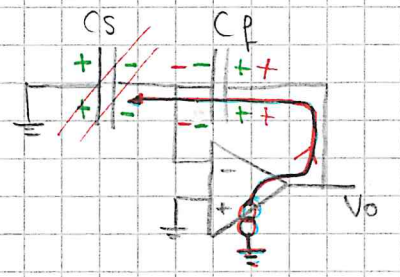
$C_S = C_f$

We want to implement $V_{RES} = 2[V_{IN} - V_{DAC}]$ (1)

ϕ_1 : $S_{1,4}$ short, $S_{2,3}$ are closed towards V_{IN}



ϕ_2 : Suppose DAC out is 0V

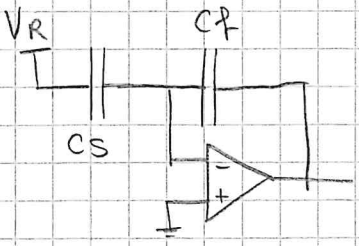


@ $t = 0^-$ both C_f, C_S stored V_{IN} as charges in color

@ $t = 0^+$ C_S is shorted by vgnd and gnd, charges move (color)

Result is $V_{OUT} \cdot C_f = V_{IN}[C_S + C_f] \rightarrow \underline{V_{OUT} = \left[1 + \frac{C_S}{C_f}\right] V_{IN} = 2V_{IN}}$ ($C_S = C_f$)

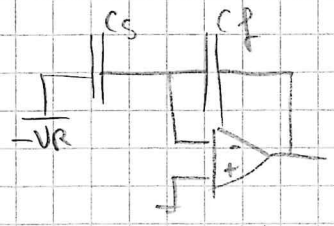
ϕ_2 : Suppose DAC out is $+V_R$. By applying the superposition of effect



$$\underline{V_{OUT}} = V_{IN}\left(1 + \frac{C_S}{C_f}\right) - V_R \frac{C_S}{C_f}$$

$$= 2V_{IN} - V_R = 2\left[V_{IN} - \frac{V_R}{2}\right]$$

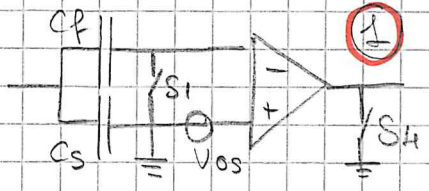
ϕ_2 : Suppose DAC out is $-V_R$:



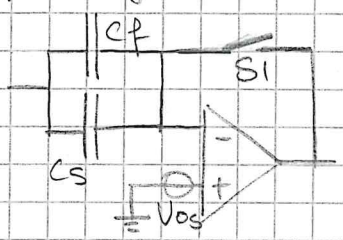
$$\underline{V_{OUT}} = 2V_{IN} + V_R - \underline{2\left[V_{IN} + \frac{V_R}{2}\right]}$$

We can see that this circuit indeed implements (1)

Let's see what happens to the opamp's offset. We can proceed in two ways of placing S_1:



① Closed S_1, S_4 (no offset removal)



② Connecting the opamp as buffer removes the offset

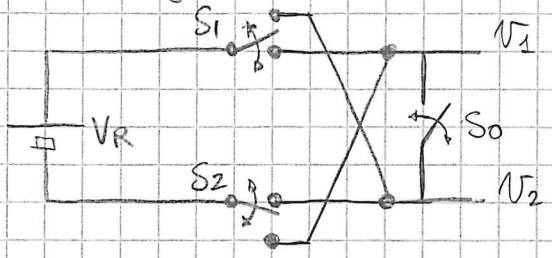
Pros/cons of ①

+ We have higher speed wrt ② because opamp is in open loop and it does not need any Miller compensation
+ Shunts Cs, Cf directly into the real ground
- Does not sample the offset
- S_4 is needed because OL operation will either unlike it go to 0/V_{DD} depending on Vos. S_4 represents a situation in which V_{OUT} is kept in a balanced point in Φ_2 (so it does not really need to be a real switch)

Pros/cons of ②

+ Samples and cancels Vos
- We sacrifice BW because of the loop compensation needed

DAC design



DAC design is trivial:

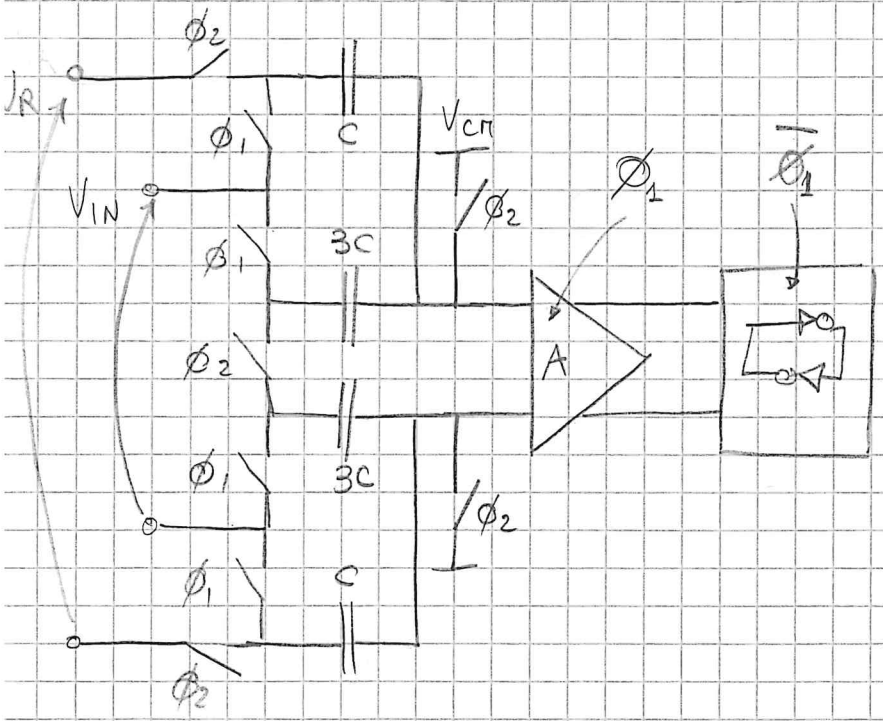
- $\pm V_R$ is obtained on V_1, V_2 by inverting the connection with the two SPDT switches $S_{1,2}$
- 0V is obtained by shorting V_1 and V_2 together with S_0

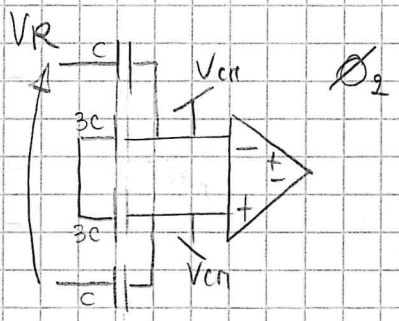
This means that V_R can be highly linear (e.g: BGR) and therefore $+V_R = |-V_R|$ because they come from the same source

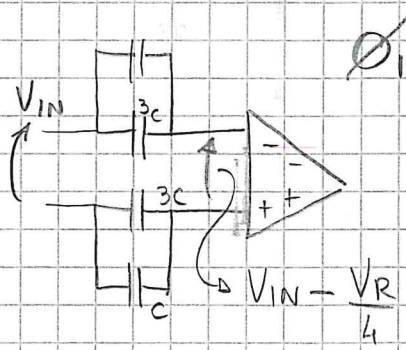
Comparator design

We solved Vos problem thanks to redundancy. However we need $\pm V_R/4$ generation and reverse isolation for kickback.

C is selected based on noise, charge sharing of C/3C generates $\frac{V_R}{4}$:

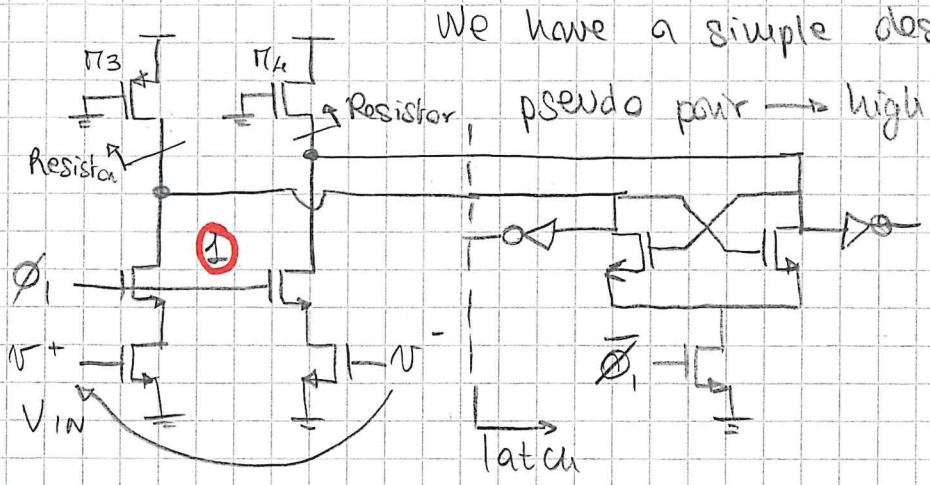






Note that we must take care of the common mode voltage of the circuit

Preamp + latch design



We have a simple design that uses a pseudo pair → high offset but we don't care because of redundancy!

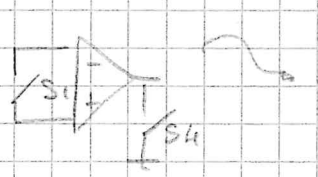
$M_{3,4}$ are resistive loads

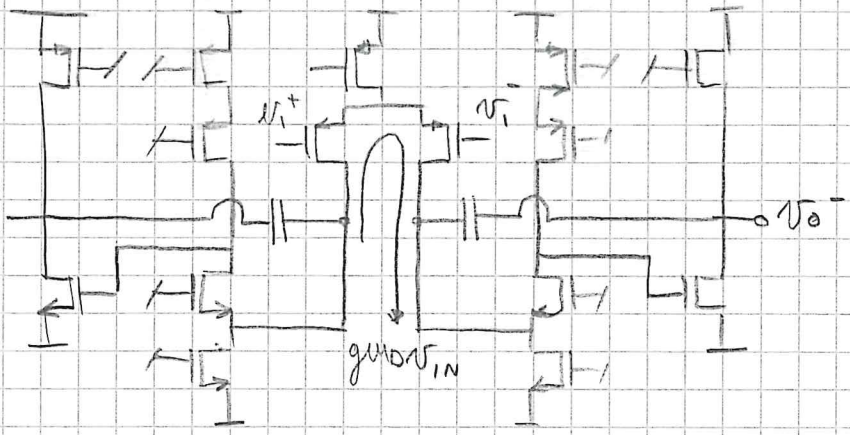
(1) is probably used to disconnect the latch for kickback.

Probably, the pseudopair is used not to have a floating current generator when (1) disconnects the pair. Could also be because of less power dissipated w/o tail generator.

Opamp design

pMOS are sometimes used for input stages for lower 1/f noise





nMOS input

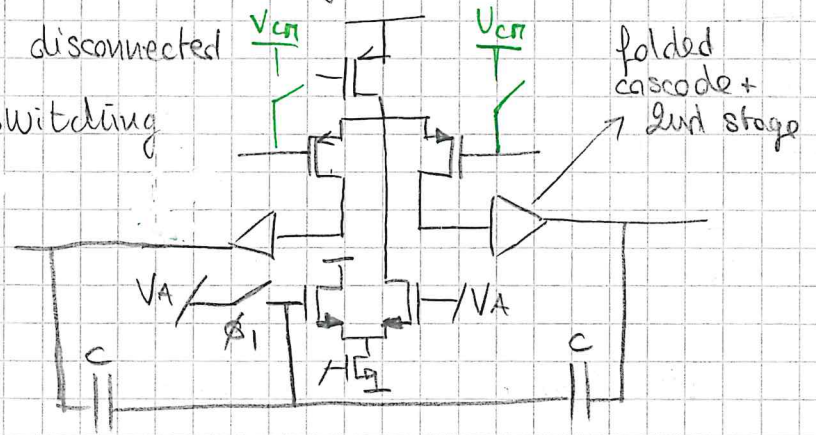
2 stage

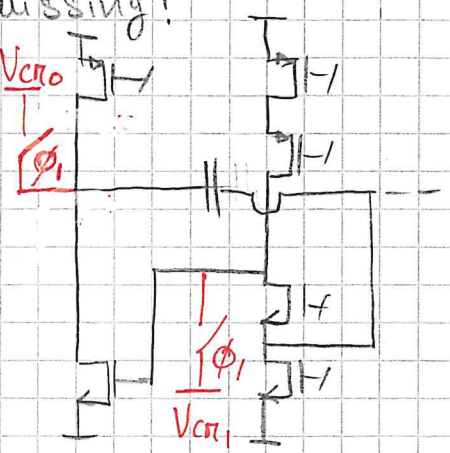
folded cascode

1st stage gain $\sim g_m r_o^2$ 2nd stage gain $\sim g_{m_o} r_{out}$

Compensation is Ahuja. CMF and S_1, S_4 are missing!

CMF is disconnected when switching

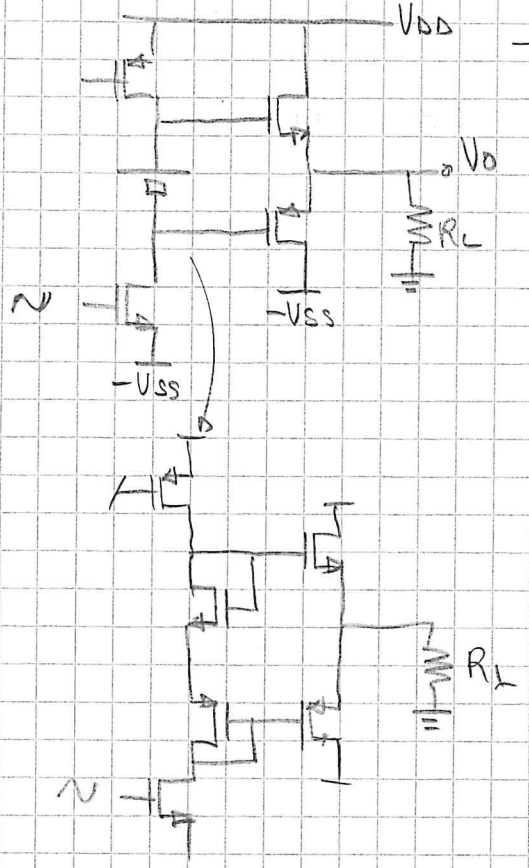




We need to short both 1st and 2nd stage outputs in order to properly generate a "balanced" state when switching

#5 | Recall on push-pull output stage

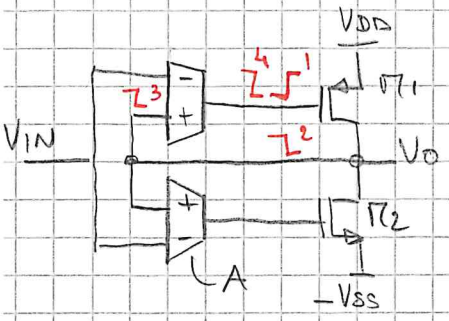
There is the usual trade-off between power/distortion.



→ push-pull. It worked fine for BJT but it's bad for CMOS. cons:

- Vo limited by large V_{GS}
- V_{GS} changes a lot because output current is high ($\sqrt{\cdot}$ vs $\ln(\cdot)$ of bipolar)
- Extra drop given by the large source increase on the body diode of the MOS

6) Alternative output stage

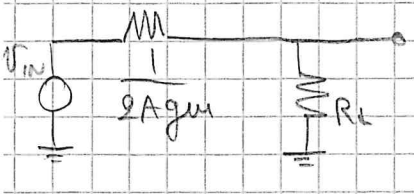


Swing here is much larger ($V_{DD} - V_{OV}$ and $-V_{SS} + V_{OV}$).

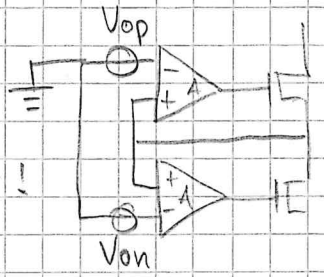
$\left.\frac{V_O}{V_{IN}}\right|_{ID} = 1$ trivial $\quad A = g_{m_{OTA}} r_{o_{OTA}}$

$$Z_{OUT} = r_{o1} // r_{o2} // \frac{1}{A(g_{m1}+g_{m2})} \simeq \frac{1}{A(g_{m1}+g_{m2})}$$

We can build a Thevenin eq.:



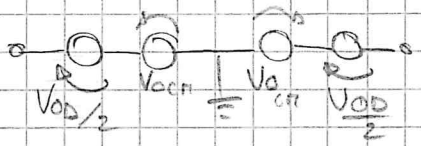
$\frac{V_O}{V_{IN}} = \frac{R_L}{R_L + \frac{1}{2Ag_m}}$ ⇝ Real gain



Issue: V_{OS} of the OTA will have an effect!

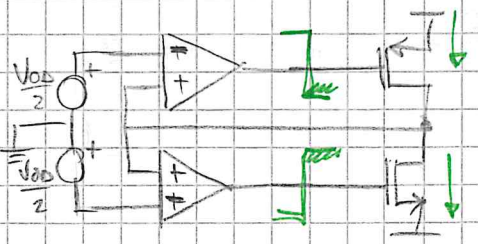
We can divide in DME and CME:

$V_{O\,CM} = \frac{V_{op} + V_{on}}{2}$ $\quad V_{O\,DIFF} = V_{op} - V_{on}$



V_{OCM} is exactly like V_{IN}:

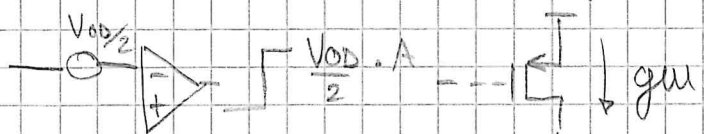
$$V_{OUT}\Big|_{RE} = \frac{V_{IN} \pm V_{OCM}}{1 + \frac{1}{2g_m A R_L}}$$



V_{OD} is a different story ⟶

We end up increasing the output bias current. We waste current for nothing and we can't control its value and feedback does not correct it. If V_{DD} is large enough, we end up with out-of-spec g_m values.

A brute force solution is to limit A so that V_{OD} does not switch ON M_1 and M_2 completely



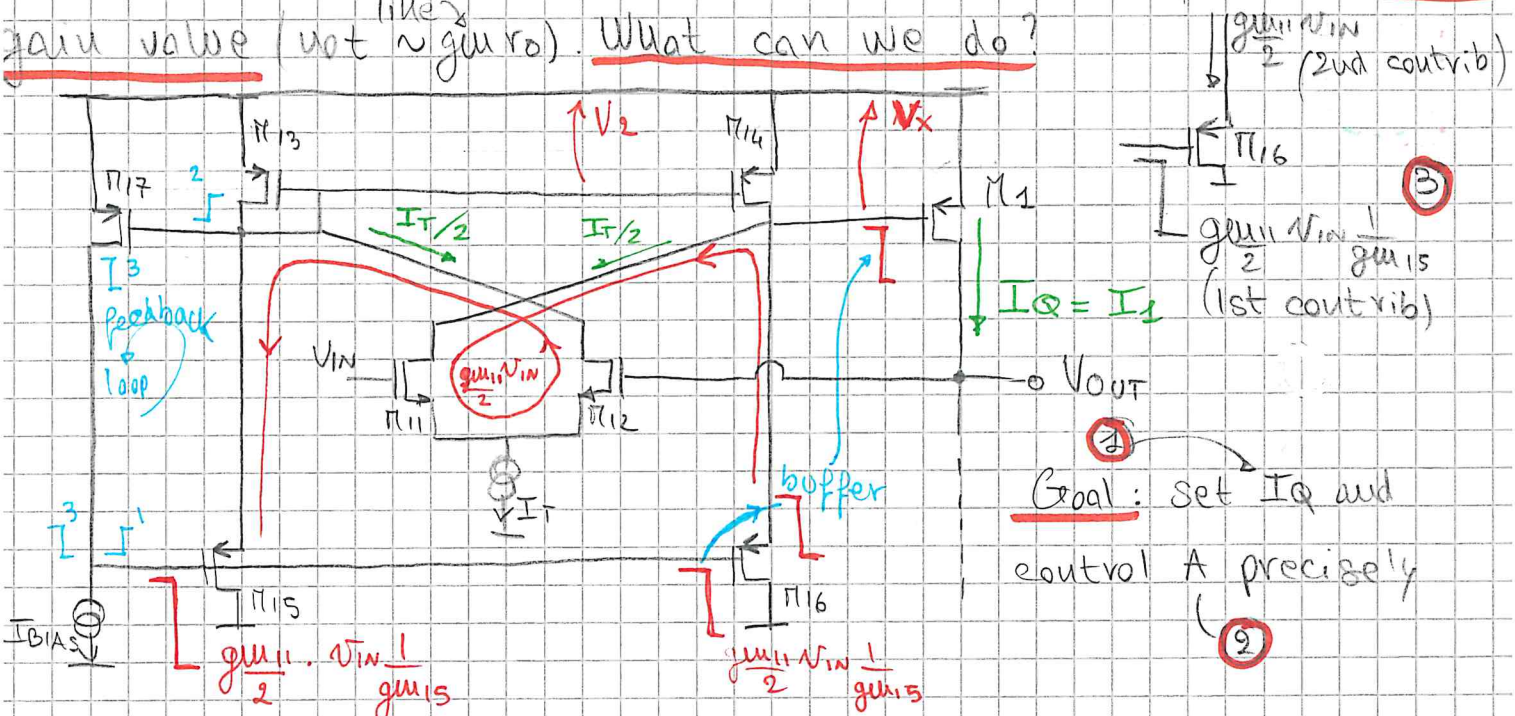
$\Delta I_Q = \frac{2 I_Q}{V_{OV1}} \cdot A \frac{V_{DD}}{2}$ where I_Q = nominal bias current w/o $V_{DD}/2$

$\frac{\Delta I_Q}{I_Q} \propto \frac{V_{DD}}{V_{OV1}} A$ ⇝ the relative error is strongly dependent on A and V_{OV}

Amp stage design

$\frac{\Delta I_Q}{I_Q} = \frac{V_{OS}}{V_{OV_1}} A$ ⇝ e.g: 20% error max, $V_{OS} = 5mV$, $V_{OV_1} = 200mV$

→ $A < 8$ ⇝ we need to precisely control the gain value (not ~~like~~ ~ $g_m r_o$). What can we do?



- I_{BIAS} is pushed into M_{17} because of the local fdback with M_{15}, M_{13} and M_{17}
- This way we set M_{13} current as well because $V_{GS13} = V_{GS17}$

$$I_{D13} = \frac{(W/L)_{13}}{(W/L)_{17}} I_{D17} = I_{D14}$$

Because of symmetry between $M_{13,14,15,16}$ also M_{14} is biased with the same $I_{D14} = I_{D13}$

It follows that $I_{D1} = I_Q = \frac{(W/L)_1}{(W/L)_{17}} I_{BIAS}$ → Solved (1)

Consider $g_{m15} = g_{m16}$

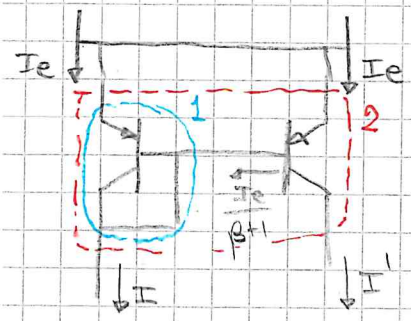
- $\frac{g_{m11}}{2} V_{IN}$ current can't go in M_{13} because $V_{GS13} = V_{GS17} = V_{GS14}$ are fixed by the feedback loop and I_{BIAS}. Since $r_{o|I_{BIAS}} \to \infty$ $G_{loop\,local} \to -\infty$ therefore all $\frac{g_{m11}}{2} V_{IN}$ goes into M_{15} → $\frac{g_{m11}}{2} V_{IN} \cdot \frac{1}{g_{m15}}$ drop on M_{15} gate → $G = \frac{V_x}{V_{IN}} = \frac{g_{m1}}{2} \cdot \frac{1}{g_{m15,16}} \cdot 2$ (3)

↳ Solved (2)

Gain is easy to control because it's just a g_m ratio

The double contribution (3) is given by the superposition of effects and gate voltage and diff current on M_{16})

Additional: bipolar current mirror using nodes



equation on node 1:

$$I_e + \frac{I_e}{\beta+1} = I \quad (1)$$

equation on node 2:

$$I_e + I_e = I + I' \quad (2)$$

If we combine (1) + (2) we immediately get $I' = I \frac{\beta}{\beta+2}$

This can be also powerful to check other mismatches

(e.g: if $I_{S1} \neq I_{S2} \rightarrow I_{C1} \neq I_{C2}$ since $V_{BE1} = V_{BE2}$)

Mixed Signal Circuits Design

8 Febbraio 2023

Giustificare tutti i risultati indicando tutti i passaggi. Indicare sempre a quale transistore ci si riferisce (e.g. la transconduttanza di Q1 è g_{m1}, la r_0 di Q2 è r_{02} il β di Q3 è β_3 etc...).

i) Calcolare l'impedenza differenziale di ingresso. Calcolare quindi il guadagno di transconduttanza $I_{out}/(V_{in}^+ - V_{in}^-)$. Si assuma $\beta_n = 3\beta_p$.

ii) Calcolare il generatore serie (di tensione) di rumore in ingresso, considerando solo il contributo del rumore shot di collettore, di tutti i trasistori.

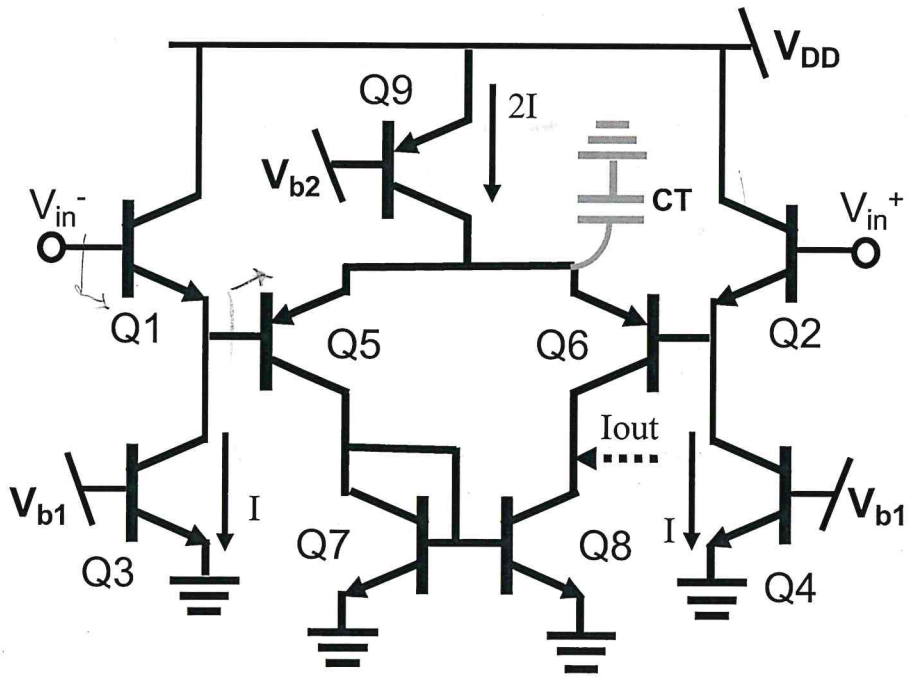
iii) Ripetere il calcolo, considerando il contributo del rumore termico della resistenza di base ($4kTr_{bb'}$) di tutti i trasistori. Assumere la stessa $r_{bb'}$ per tutti i transistori.

iv) Ricavare la condizione riguardante la corrente I (una disuguaglianza) per cui questo secondo termine può essere trascurato rispetto al precedente, sapendo che $r_{bb'} = 200\ \Omega$ (assumere la temperatura ambiente).

v) Calcolare l'offset di ingresso dovuto al mismatch delle correnti di saturazione della coppia Q1-Q2 (assumere $+\Delta Is/2$ e $-\Delta Is/2$). Ripetere lo stesso calcolo per la coppia Q7-Q8.

vi) Calcolare il trasferimento tra un segnale di modo comune in ingresso e la corrente di segnale di uscita, $2I_{out}/(V_{in}^+ + V_{in}^-)$, in continua, dovuto solo all'errore di specchiamento (dovuto al β_n finito).

vii) Ripetere il calcolo ad "alta" frequenza, ossia considerando l'effetto di C_T. Tracciare i diagrammi di Bode (modulo e fase) quotati della funzione di trasferimento completa.



Mixed Signal Circuits Design

8 Febbraio 2023

Always justify the results, indicating all the steps (do not provide only the results). Always indicate at what transistor you are referring to (e.g. the transconductance of Q1 is g_{m1}, r_0 of Q2 is r_{02}, β of Q3 is β_3 etc...).

i) Evaluate the input differential impedance. Calculate the transconduttance gain, i.e. $I_{out}/(V_{in}^+ - V_{in}^-)$. Assume $\beta_n = 3\beta_p$.

ii) Evaluate the equivalent series (voltage) noise generator, considering only the contribution from the current collector shot noise sources for all the transistors.

iii) Repeat the previous evaluation, considering only the thermal noise from the base resistance ($4kTr_{bb'}$) for all the transistors. Assume the same $r_{bb'}$ for all the transistors.

iv) Derive the condition (an inequality) for the current I for which the second contribution is negligible with respect to the previous one, assuming $r_{bb'}$ = 200 Ω (assume room temperature).

v) Calculate the input offset due to the mismatch of the saturation currents (assume $+\Delta Is/2$ and $-\Delta Is/2$). Repeat the same calculation for the couple Q7-Q8.

vi) Evaluate the DC gain between an input common mode voltage signal, and the output current, i.e. $2I_{out}/(V_{in}^+ + V_{in}^-)$, due to the error in the mirror (due to the finite β_n).

vii) Repeat the same evaluation at "high" frequency, that is considering the effect of C_T. Plot the Bode diagrams (magnitude and phase) of the entire transfer function.